WB32F10x
PCB Layout Suggestions

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Contents

1 Printed Circuit Board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (VSS) and another dedicated to the VDD supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

2 Component Position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution in order to reduce cross-coupling on the PCB, that is noisy, high-current circuits, low-voltage circuits, and digital components

3 Ground And Power Supply (VSS/VDD)

Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually and all ground returns should be to a single point. Loops must be avoided or have a minimum area. The power supply should be implemented close to the ground line to minimize the area of the supply loop. This is due to the fact that the supply loop acts as an antenna, and is therefore the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low an impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors C (100nF) and a chemical capacitor C of about 10µF connected in parallel on the WB32F10xxx device. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10nF to 100nF, but exact values depend on the application needs. *Figure 1*shows the typical layout of such a VDD/VSS pair.

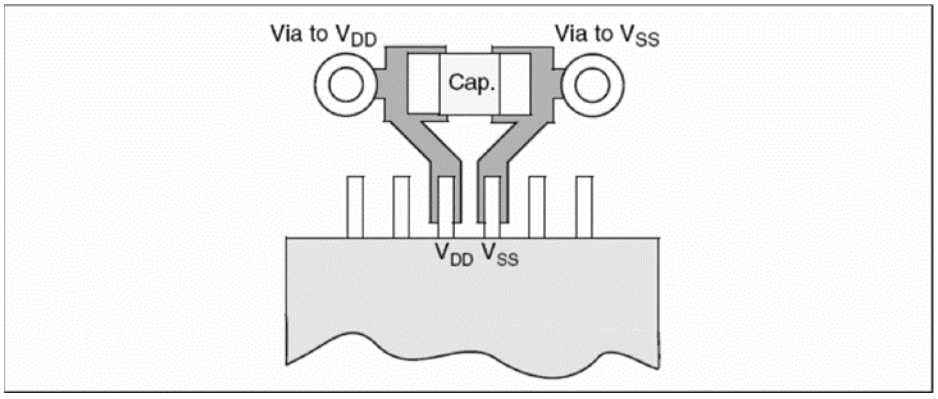


Figure 1 A typical layout of VDD /VSS

5 Power supply schemes

The circuit is powered by a stabilized power supply, VDD

- **Note**
  - If the ADC is used, the VDD range is limited to 2.4 V to 3.6 V
  - If the ADC is not used, the VDD range is 2.0 V to 3.6 V
- The VDD pins must be connected to VDD with external decoupling capacitors (one 100nF Ceramic capacitor for each VDD pin + one Tantalum capacitor (min. 4.7 µF typ.10 µF)
- VBAT pins must be connected to External battery (1.8V < V_{BAT} < 3.6V)。If no external battery is available, the VBAT must be connected to VDD through a 100nF Ceramic Capacitor.
- VDDA pin must be connected to 2 external decoupling capacitors.(10nF Ceramic Capacitor +1uF Tantalum)
- VREF+ pin can be connected to VDDA.If a separate external reference is used on VREF+, a 10nF and a 1µF capacitor must be connected to VREF+. In all cases, VREF+ must be between 2.4V and VDDA

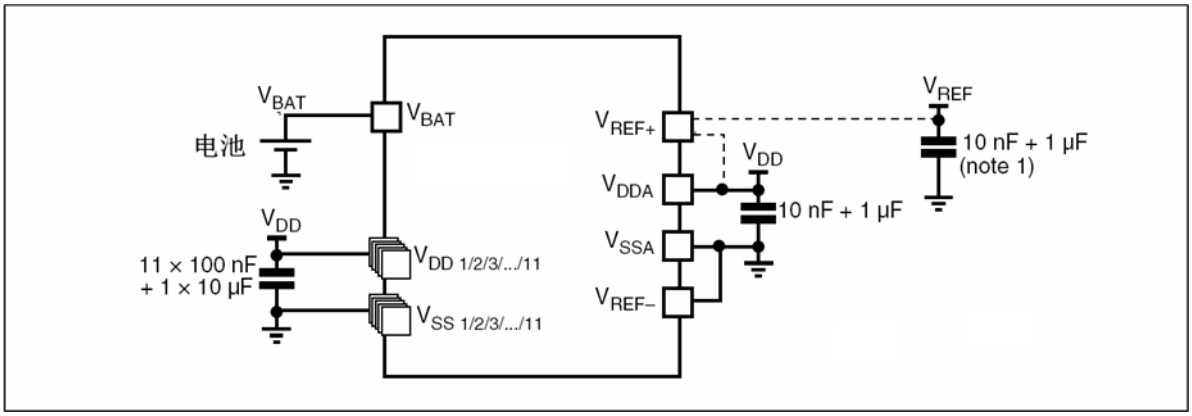


Figure 2 Power Supply Scheme

6 Other Signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (the case of interrupts and handshaking strobe signals, and not the case for LED commands).
- For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
- For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- The 3W principle should be met as far as possible, and the adjacent traces should be kept as far away as possible to reduce coupling and interference.If ADC and CMP require high precision, they must be surrounded by GND.
- Noisy signals (clock, etc.)
- Sensitive signals (high impedance, etc.)

7 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance, unused clocks, counters or I/Os, should not be left free, e.g. I/Os should be set to “0” or “1”(pull-up or pull-down to the unused I/O pins.) and unused features should be “frozen” or disabled.

8 CLOCK

LSE route should be as far away from HSE route as possible.

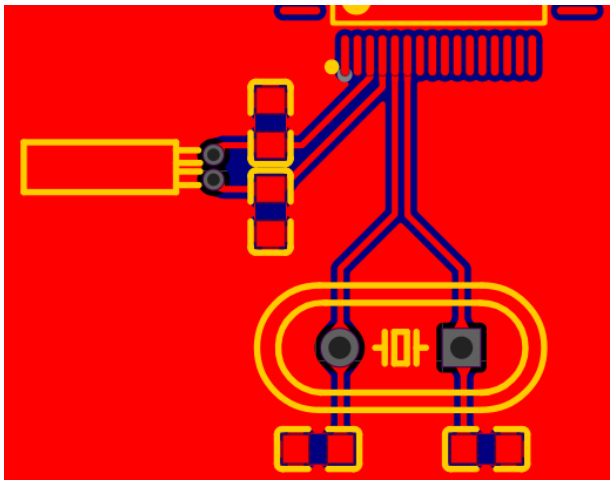


Figure 3 LSE and HSE wiring

9 Analog Signal

In order to improve the sampling accuracy, the analog signal of ADC channel needs to be isolated from the digital signal, and it needs to be grounded and shielded.

10 EMI

1. Make sure the power supply is rated for the application and optimize with decoupling capacitors.

2. Provide adequate filter capacitors on the power supply. Bulk/Bypass and Decoupling Capacitors should have Low Equivalent Series Inductance (ESL)

3. All empty PCB wiring areas need to be connected to ground(GND), and all ground planes need to be connected together.

4. 4Bypass every power input to board with a high-frequency capacitor

5. Differential signal line must be matched in length, or it will cause timing skew, reduce signal quality, and increase EMI.

6. Differential signal lines need to be routed on the same PCB layer, because differences in impedance and vias between different layers will reduce the effect of differential-mode signal transmission and introduce common-mode noise.

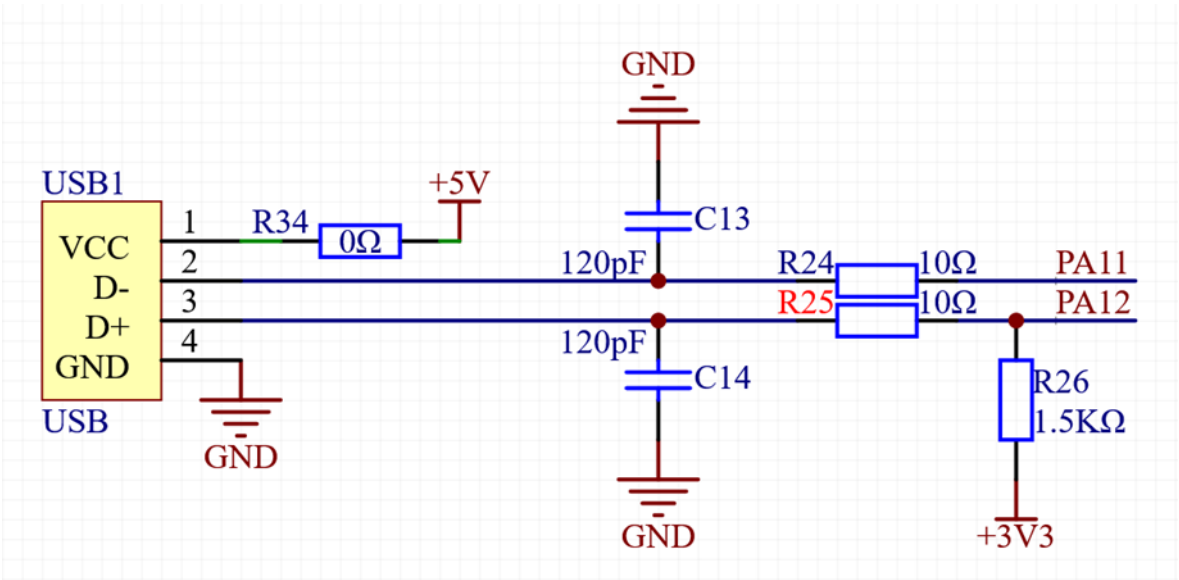
7. High-speed signal lines should not have vias, the ground plane on the back should be complete, and the traces should be as short as possible, keeping a distance from other signal lines. If the usb interface needs series terminal resistors or USB D+/D- needs to be connected with pull-up resistors, be sure to place these resistors as close to the chip as possible.

8. Every VDD pins of MCU with two high-frequency capacitor (Tpy. 1uF and 0.1Uf).

9. Add small damping resistors(10R) or ferrites(120pf) to SPI or IIC clock outputs and keep hot leads short.

10. The line of the crystal oscillator needs to be as short as possible, and the signal line should not be routed on the back of the crystal oscillator. If the layout allows, try placing vias around the crystal to ground(GND) to ensure the integrity of the ground plane around the crystal.

1 USB schematic design reference



Revision history

Revision	Date	Description
1.0	2019/12/15	Initial Release
1.4	2022/06/30	Added EMI section and USB schematic design reference

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