4-Kbit Serial Presence Detect (SPD) EEPROM Compatible with JEDEC EE1004-v for DIMM

DATASHEET Rev.1.2

Features

- Supply Voltage: 1.7V to 3.6V
- JEDEC EE1004-v Serial Presence Detect (SPD) Compliant
- 2-wire Serial Interface I^2C/SMBus Compatible
  - 1MHz (Maximum) Supported in Full Supply Voltage Range
  - Bus Timeout Supported
- Software Write Protection on All Four 128-byte Blocks
- Byte and Page (up to 16 Bytes) Write Mode
  - Partial Page Writes Allowed
- Self-timed Write Cycle: 2ms (typical)
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High Reliability
  - Endurance: 5,000,000 Write Cycles
  - Data Retention: 100 Years
- Low Operating Current
  - Write Current: 0.2mA (typical)
  - Read Current: 0.2mA (typical)
  - Standby Current: 0.1μA (typical)
- Operating Temperature Range: -40°C to +105°C
- Green Packaging Options (Pb/Halide-free/RoHS Compliant)
  - 8-lead TSSOP, 8-pad UDFN and 8-pad WDFN

Description

The WB34C04 is a 4-Kbit EEPROM device designed to be fully compatible to industrial standard I^2C/SMBus interface and compliant to the JEDEC EE1004-v specification. The device is designed to operate in a supply voltage range of 1.7V to 3.6V, with a maximum of 1MHz transfer rate. The operating temperature range is from -40°C to +105°C. A bus Timeout feature is supported to prevent system lock-ups.

The Serial EEPROM memory is organized as four blocks of 128 bytes each. Each block is comprised of eight pages of 16 bytes each. The Serial EEPROM operation is tailored specifically for Dual Inline Memory Modules (DIMM) with Serial Presence Detect (SPD) to store a module's vital product data such as size, speed, voltage, data width, and timing parameters.

The WB34C04 incorporates a Software Write Protection feature enabling the capability to selectively write protect any or all of the four 128-byte blocks. Once the write protection is set, it can only be reversed by sending a specific sequence and the write protection for all blocks is cleared simultaneously.

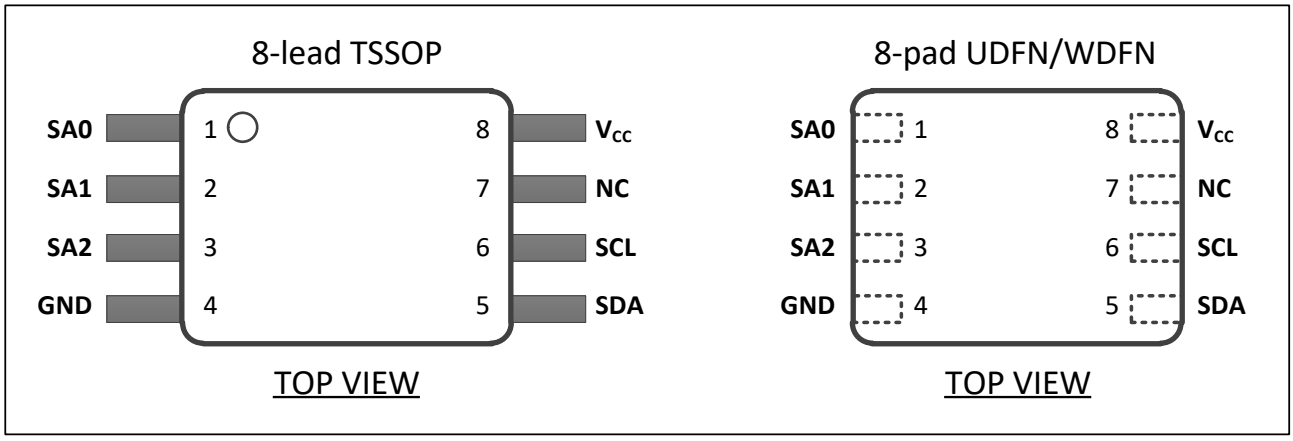
Table of Contents

1 Pin Descriptions and Pin Configuration

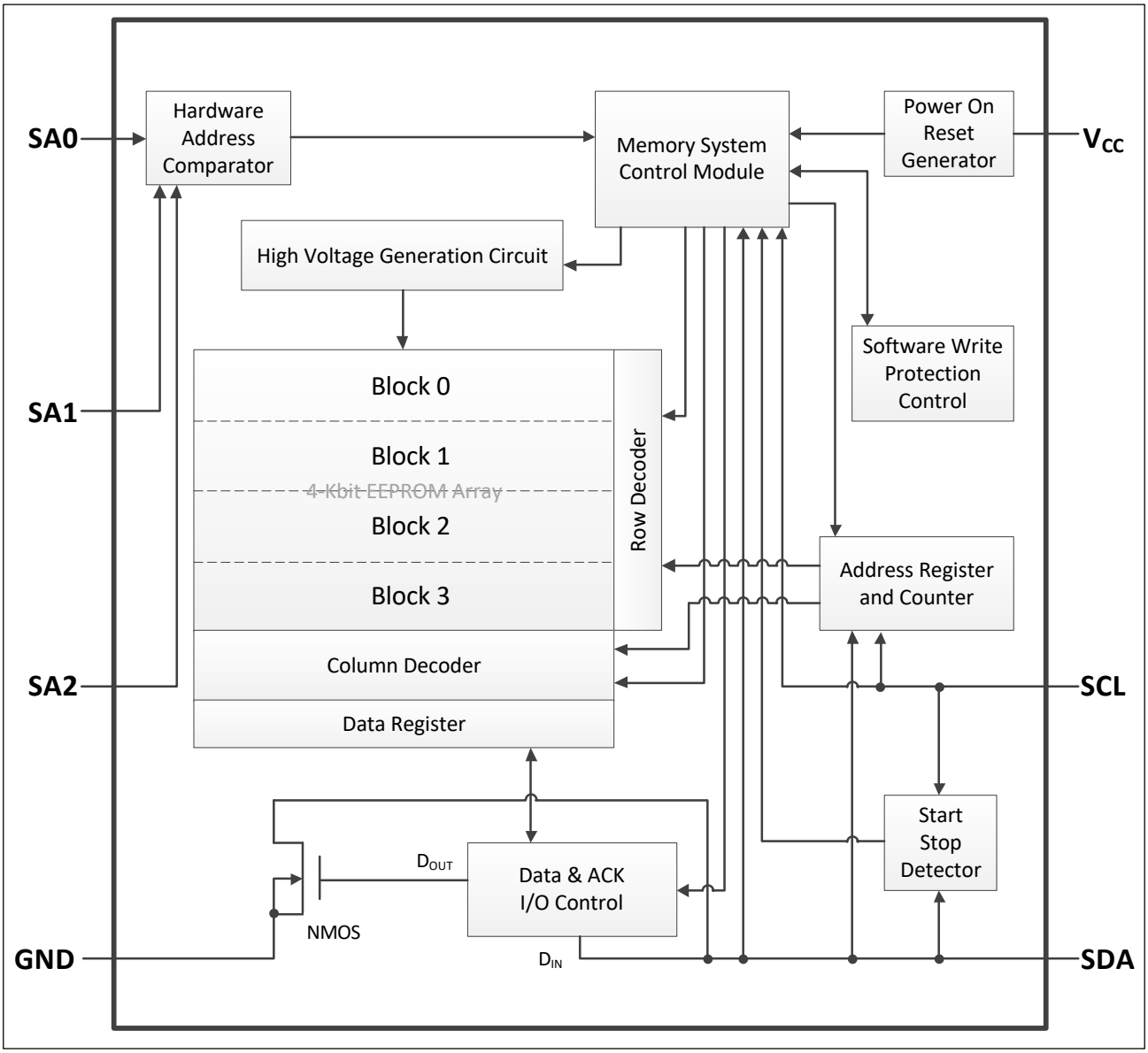
Table 1–1 Pin Descriptions

Symbol	Type	Name and Function
SA0 SA1 SA2	Input	**Device Address Inputs:** The SA0, SA1, and SA2 pins are used to select the device address and correspond to the three Least Significant Bits of the I^2C/SMBus seven-bit slave address. These pins can be directly connected to V_{CC} or GND in any combination, allowing up to eight devices on the same bus. The SA0 pin is also used to detect the V_{HV} voltage, when decoding a SWPn or CWP instruction. See **Table 6–1** for decode details.
SDA	Input/Output	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device.
SCL	Input	**Serial Clock:** The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL.
V_{CC}	Power	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.
GND	Power	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.
NC	---	**No Connection:** The NC pin is not bonded to a die pad. This pin can be connected to GND or left floating.

Figure 1–1 Pin Configuration



2 Functional Block Diagram



3 Device Communication

The WB34C04 operates as a slave device and utilizes a 2-wire serial interface to communicate with the Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). Data is always latched into the WB34C04 on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL pin and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

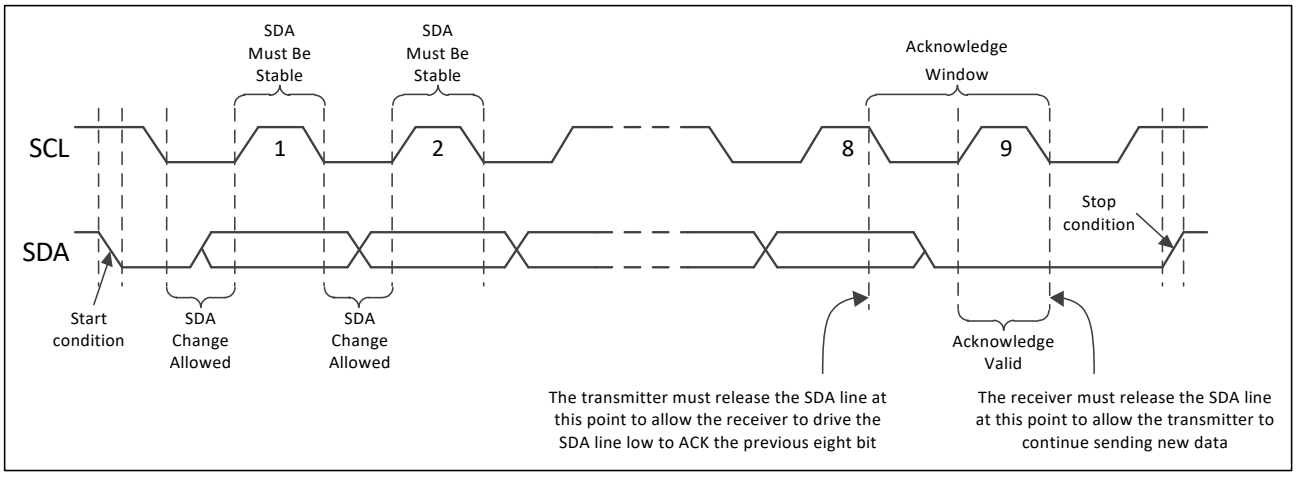
All command and data information is transferred with the Most Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after eight bits of data has been transferred, the receiving device must respond with an acknowledge or a no-acknowledge response bit during a ninth clock cycle generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There is no unused clock cycle during any Read or Write operation, so there must not be any interruptions or breaks during the data stream.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

3.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in Logic 1 state. The Start condition must precede any command as the Master uses a Start condition to initiate any data transfer sequence (see **Figure 3–1**). The WB34C04 will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given.

Figure 3–1 Start, Stop, and ACK



3.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in Logic 1 state (see **Figure 3–1**). A stop condition terminates communication between the WB34C04 and the Master. A Stop condition at the end of a Write command triggers the EEPROM internal write cycle. Otherwise, the WB34C04 subsequently returns to Standby mode after receiving a Stop condition.

3.3 Acknowledge (ACK)

After each byte of data is received, the WB34C04 should acknowledge to the Master that it has received the data byte successfully. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the WB34C04 must output Logic 0 as ACK for the entire clock cycle so that the SDA line must be stable in Logic 0 state during the entire high period of the clock cycle (see **Figure 3–1**).

3.4 No-Acknowledge (NACK)

When the WB34C04 is transmitting data to the Master, the Master can indicate that it is done receiving data and end the operation by sending a NACK response to the WB34C04 instead of an ACK response. This is accomplished by the Master outputting Logic 1 during the ACK/NACK clock cycle, at which point the WB34C04 should release the SDA line so that the Master can then generate a Stop condition.

3.5 Standby Mode

The WB34C04 features a low-power Standby mode which is enabled:

- Upon power-up *or*
- After the receipt of a Stop condition and the completion of any internal operations.

3.6 Device Reset and Initialization

The WB34C04 incorporates an internal Power-On Reset (POR) circuit to prevent inadvertent operations during power-up. On a cold power-up, the device does not respond to any instructions until the supply voltage reaches the internal reset threshold voltage (V_{POR}). The supply voltage must rise continuously between V_{POR} and V_{CC}(Min) without any ring back to ensure a proper power-up (see **Figure 3–2**). Once the supply voltage passes V_{POR}, the device is reset and enters Standby mode. However, no protocol should be issued to the device until a valid and stable supply voltage is applied for the time specified by the t_{INIT} parameter. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Write instruction, until the end of the internal write cycle.
Parameters related to POR are listed in **Table 3–1**.

Figure 3–2 Power-up Timing

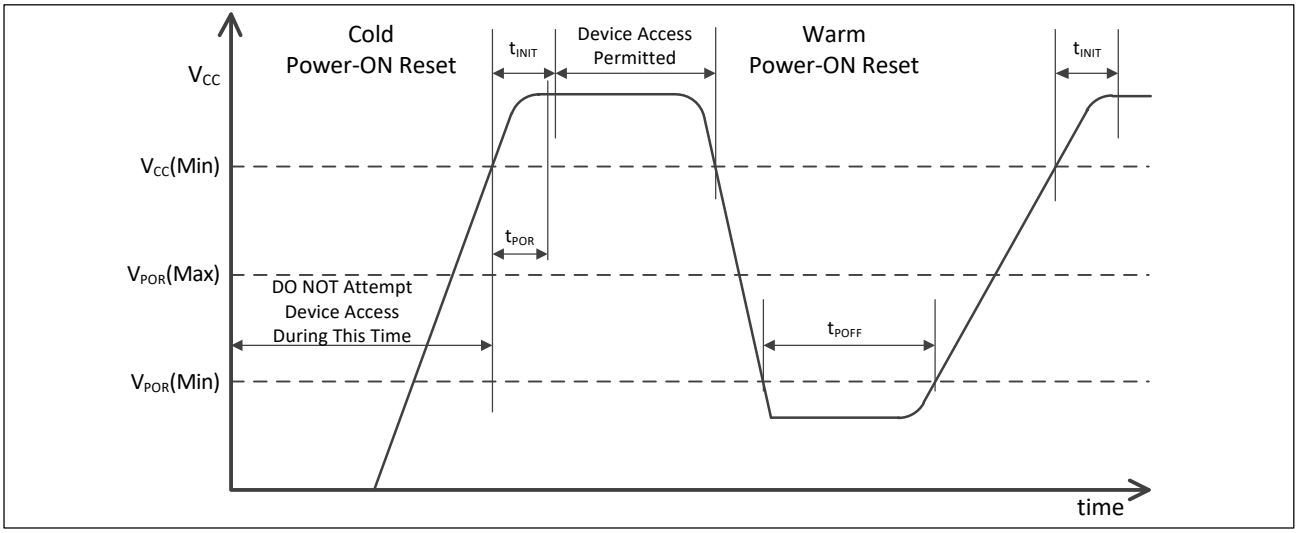


Table 3–1 Power-up Conditions

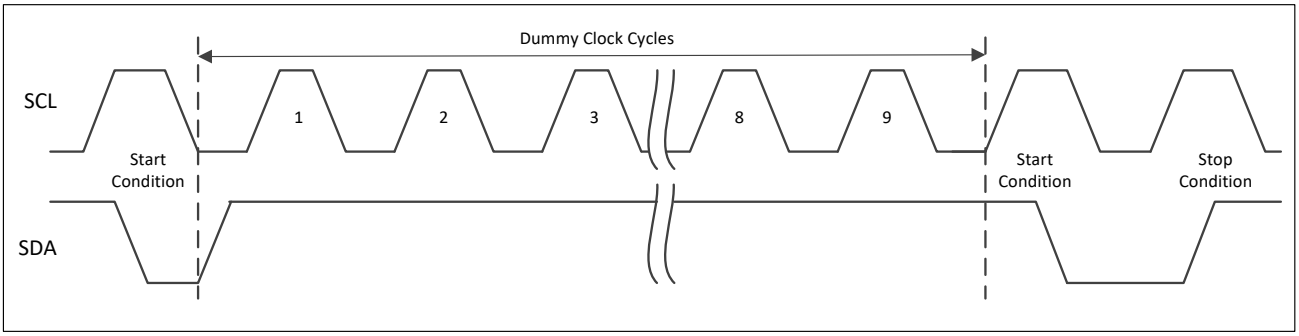
Symbol	Parameter	Min	Max	Units
t_{POR}	Power-On Reset Time		10.0	ms
V_{POR}	Power-On Reset Voltage	1.0	1.6	V
t_{INIT}	Time from Power-On to First Command	10.0		ms
t_{POFF}	Warm Power Cycle Off Time	1.0		ms

3.7 Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition.
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition (see **Figure 3–3**).

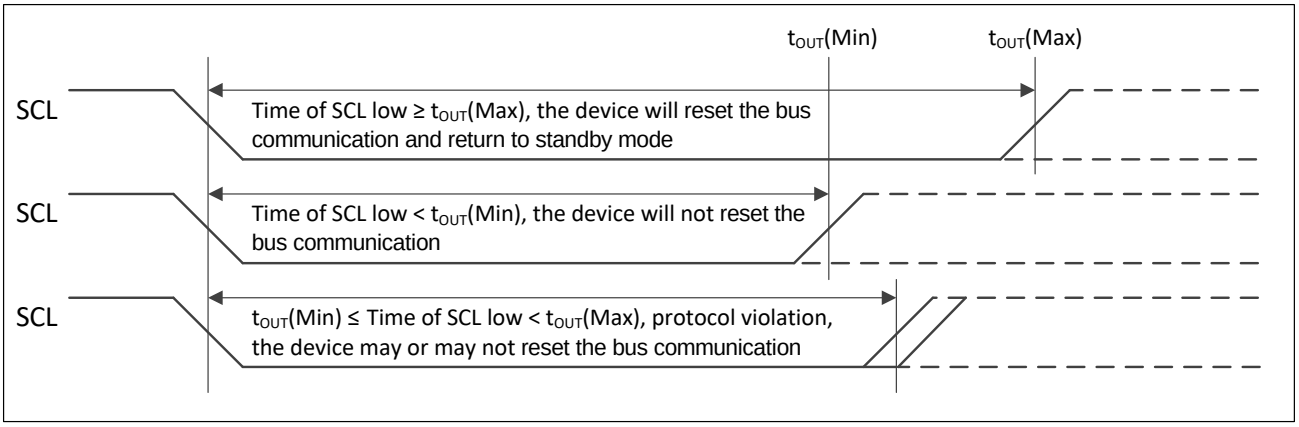
Figure 3–3 2-wire Software Reset



3.8 Timeout Function

The WB34C04 supports the industry standard bus Timeout feature to prevent potential system bus lock-ups. The device resets the serial interface and returns to standby mode if the SCL pin is held low for more than the maximum Timeout t_{OUT}(Max) specification. If the SCL pin is held low for less than the minimum Timeout t_{OUT}(Min) specification, the device will not reset the serial interface (see **Figure 3–4**). This feature requires a minimum SCL clock speed of 10kHz to avoid any timeout issues.

Figure 3–4 Bus Timeout



4 Device Addressing

The WB34C04 requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with the Serial EEPROM. The device address byte is comprised of a 4-bit device type identifier followed by three device address bits (A2, A1, and A0) and a R/$\overline{W}$ bit and is clocked by the Master on the SDA pin with the most significant bit (bit 7) first (see **Table 4–1**).

The WB34C04 will respond to two unique device type identifiers. The device type identifier of '1010' is necessary to select the device for Read or Write operation. The device type identifier of '0110' is used to access the page address function which determines what the internal address counter is set to. The device type identifier of '0110' is also used to access the Software Write Protection feature of the device.

The software device address bits (A2, A1 and A0) must match their corresponding hard-wired device address inputs (SA2, SA1 and SA0) (see **Table 4–2**), allowing up to eight devices on the bus at the same time. The eighth bit of the address byte is the R/$\overline{W}$ operation selection bit. A Read operation is selected if this bit is Logic 1, and a Write operation is selected if this bit is Logic 0. Upon a compare of the device address byte, the WB34C04 will output an ACK or a NACK during the ninth clock cycle if the compare is true or not true. The device will return to the low-power Standby Mode after a NACK.

Table 4–1 WB34C04 Device Address Byte

Function	Device Type Identifier				Device Address			Read/Write
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EEPROM Read and Write Operations	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Write Protection and Page Address Functions	0	1	1	0	A2	A1	A0	R/$\overline{W}$

Table 4–2 Device Address Combinations

Software Device Address Bits	Hard-wired Device Address Inputs		
A2, A1, A0	SA2	SA1	SA0
000	GND	GND	GND
001	GND	GND	V_{CC}
010	GND	V_{CC}	GND
011	GND	V_{CC}	V_{CC}
100	V_{CC}	GND	GND
101	V_{CC}	GND	V_{CC}
110	V_{CC}	V_{CC}	GND
111	V_{CC}	V_{CC}	V_{CC}

5 Read and Write Operations

5.1 Memory Organization

The WB34C04 memory is organized into two independent 2-Kbit memory arrays (the lower half of the memory and the upper half of the memory). Each 2-Kbit (256-byte) array is internally organized as two independent blocks of 128 bytes with each block comprised of eight pages of 16 bytes. Including both halves of the memory, there are four 128-byte blocks totaling 512 bytes (see **Table 5–1**).

The WB34C04 utilizes a Set Page Address (SPA) command and Read Page Address (RPA) command to select and verify the desired half of the memory for Write and Read operations. If SPA = 0, the lower 256 bytes of the Serial EEPROM is selected allowing access to Block 0 and Block 1. Alternately, if SPA = 1, the upper 256 bytes of the Serial EEPROM is selected allowing access to Block 2 and Block 3.

Table 5–1 SPA Setting and Memory Organization

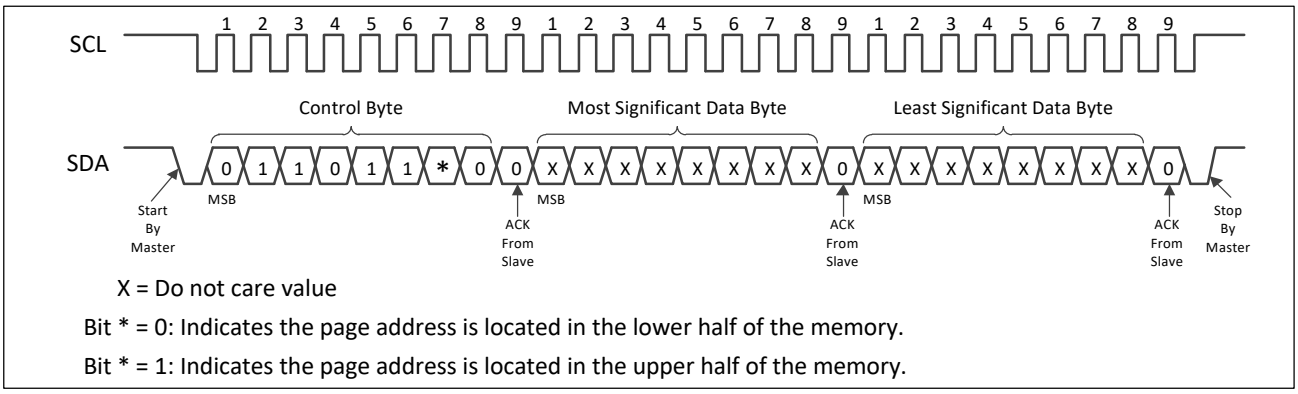
Blocks	Set Page Address (SPA)	Memory Address Locations
Block 0	0	00h to 7Fh (decimal 0 to 127)
Block 1	0	80h to FFh (decimal 128 to 255)
Block 2	1	00h to 7Fh (decimal 0 to 127)
Block 3	1	80h to FFh (decimal 128 to 255)

5.1.1 Set Page Address Command

Setting the SPA value selects the desired half of the EEPROM for Write or Read operation. The SPA command sequence requires the Master to transmit a Start condition followed by sending a control byte of ‘01101100’ or ‘01101110’. ‘0’ in the bit 7 position indicates setting the page address to the lower half of the memory while ‘1’ in this position indicates setting the page address to the upper half of the memory (see **Figure 5–1**). After receiving the control byte, the WB34C04 should return an ACK. The Master follows by sending two data bytes of Don’t Care values and the WB34C04 responds with an ACK for each of the two data bytes. The protocol is completed by the Master sending a Stop condition.

After power-up, the SPA is set to zero, indicating internal address counter is located in the lower half of the memory. Performing software reset will not change the SPA setting.

Figure 5–1 Set Page Address (SPA)

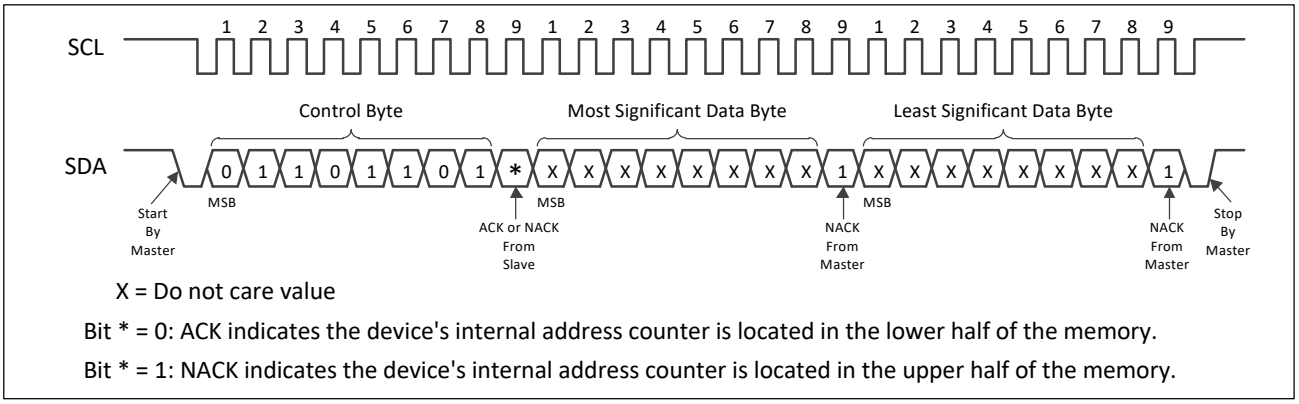


5.1.2 Read Page Address Command

Reading the state of the SPA can be accomplished by the RPA command. The RPA command sequence requires the Master to transmit a Start condition followed by a control byte of ‘01101101’. The Master

determines if the internal address counter is located in the lower half or upper half of the memory based on the device's ACK or NACK response. If the device's current address counter is located in the lower half of the memory, the WB34C04 will respond with an ACK. Alternatively, a NACK response indicates the address counter is located in the upper half of the memory (see **Figure 5–2**). Following the ACK or NACK response, the WB34C04 transmits two data bytes of Don't Care values. The Master should respond with a NACK on each of the two data bytes followed by sending a Stop condition to end the operation.

Figure 5–2 Read Page Address (RPA)



5.2 Read Operations

All Read operations are initiated by the Master transmitting a Start condition, a device type identifier of '1010', three software address bits (A2, A1, A0) corresponding to the hard-wired address pins (SA2, SA1, SA0) and the R/$\overline{W}$ select bit with Logic 1 state. In the following clock cycle, the device should return an ACK. The subsequent sequence depends on the Read operation type. There are three Read operations: Current Address Read, Random Address Read, and Sequential Read. All Read operations should be preceded by the SPA and/or RPA commands to ensure the desired half of the memory is selected.

5.2.1 Current Address Read

For a Current Address Read operation, the Master sends a Start condition followed by transmitting the device address byte with the R/$\overline{W}$ bit set to Logic 1 (see **Figure 5–3**). The WB34C04 should respond with an ACK and then serially transmits the data word addressed by the internal address counter. This address maintained by the internal address counter is the last address accessed during the last Read or Write operation. The counter is then incremented by one and the address will stay valid between operations as long as power to the device is supplied. The address roll-over during a Read operation is from the last byte of the last page to the first byte of the first page of the addressed half of the memory depending on the current SPA setting. To end the command, the Master responds with a NACK and a Stop condition.

5.2.2 Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address byte are transmitted to the WB34C04 as part of the dummy write sequence (see **Figure 5–4**). Once the device address byte and data word address are clocked in and acknowledged by the WB34C04, the Master generates another Start condition and then initiates a Current Address Read by sending another device address byte with the R/$\overline{W}$ bit set to Logic 1. The WB34C04 responds with an ACK to the device address byte and serially clocks out the first data word and

increments its internal address counter by one. The device will continue to transmit sequential data words as long as the Master continues to ACK each data word. To end the sequence, the Master responds with a NACK followed by a Stop condition.

Figure 5–3 Current Address Read

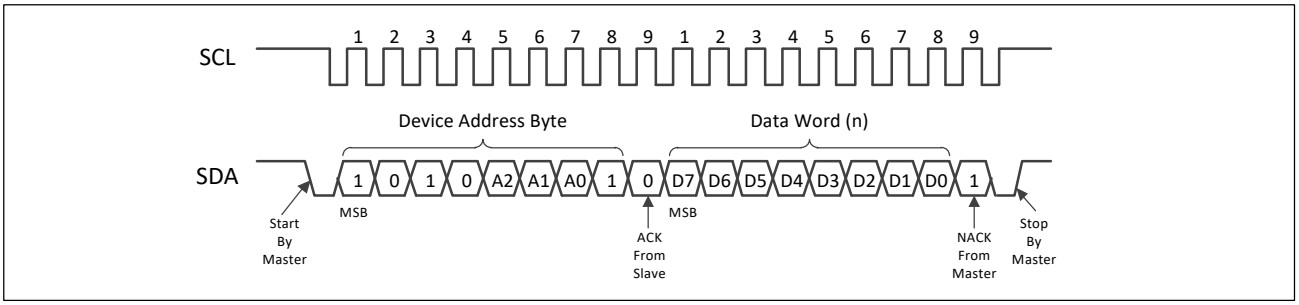


Figure 5–4 Random Read

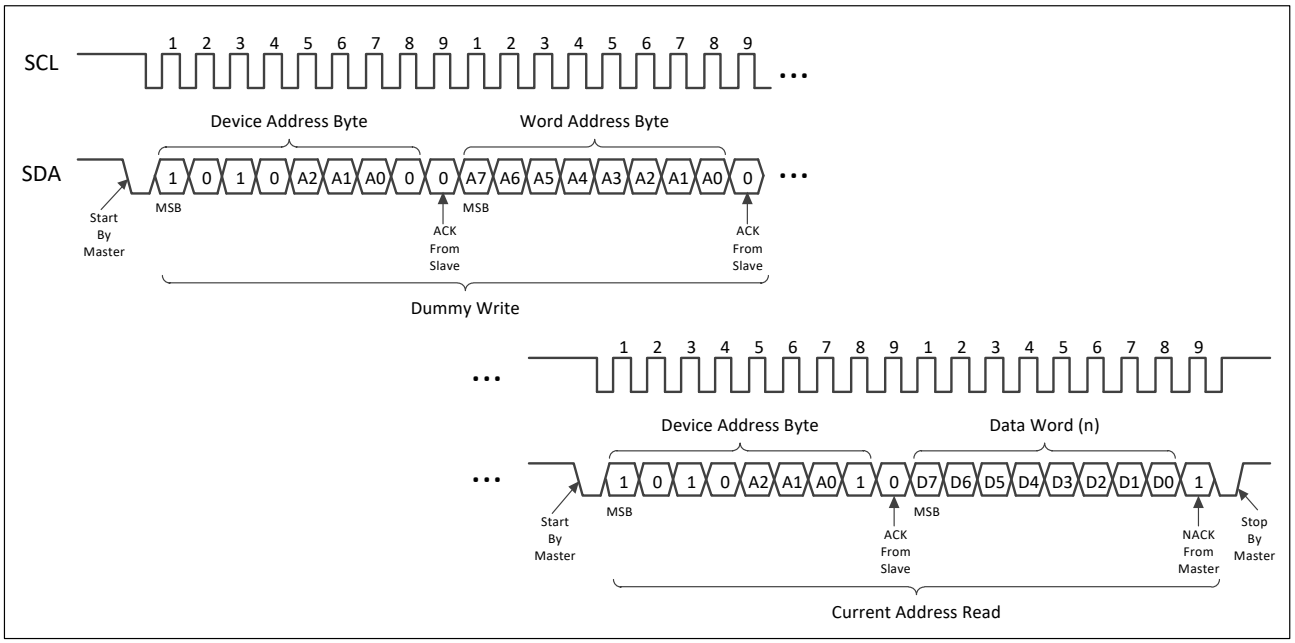
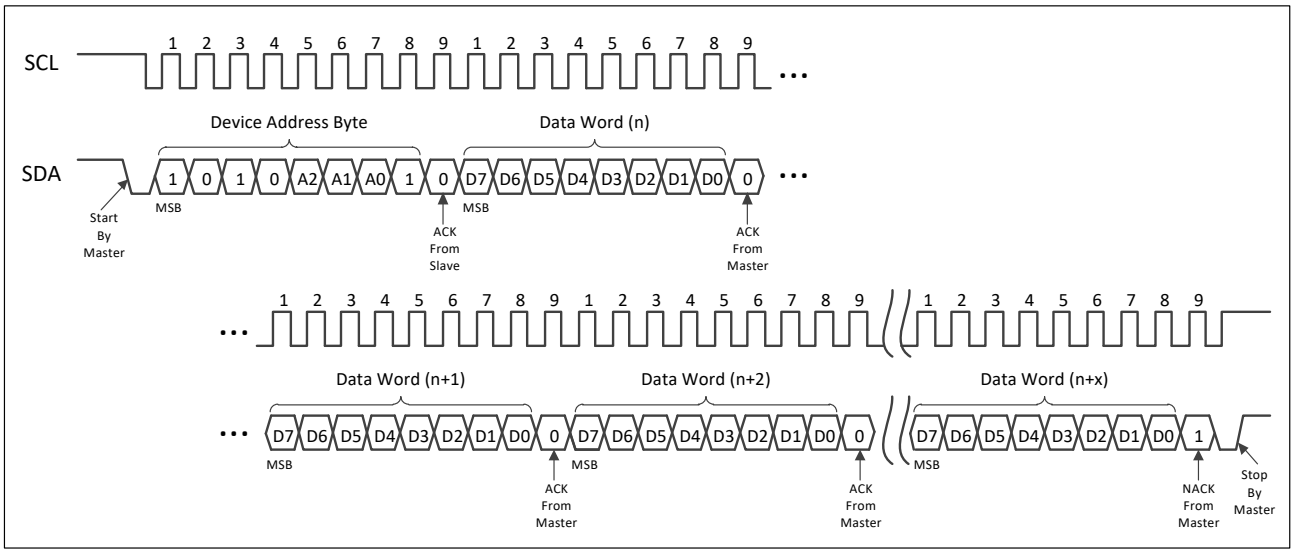


Figure 5–5 Sequential Read



5.2.3 Sequential Read

A Sequential Read operation is initiated in the same way as either a Current Address Read or a Random Read, except that after transmitted the first data word by the WB34C04, the Master responds with an ACK instead of a NACK. As long as the WB34C04 receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words (see **Figure 5–5**). When the internal address counter is at the last byte of the last page, the data word address will roll-over to the beginning of the selected half of the memory depending on the current SPA setting and the Sequential Read operation will continue. The Sequential Read operation is terminated when the Master responds with a NACK followed by a Stop condition.

5.3 Write Operations

The WB34C04 supports single Byte Write and Page Write up to the maximum page size of 16 bytes in one operation. The only difference between a Byte Write and a Page Write operation is the amount of data bytes sent to the device. Regardless of whether a Byte Write or Page Write operation is performed, the internally self-timed write cycle will take the same amount of time to write the data to the addressed memory location(s). All Byte Write and Page Write operations should be preceded by the SPA and/or RPA commands to ensure the internal address counter is located in the desired half of the memory.
If a Byte Write or Page Write operation is attempted to a Write Protected or not protected block, the WB34C04 will respond with ACK or NACK to the write operation according to **Table 5–2**.

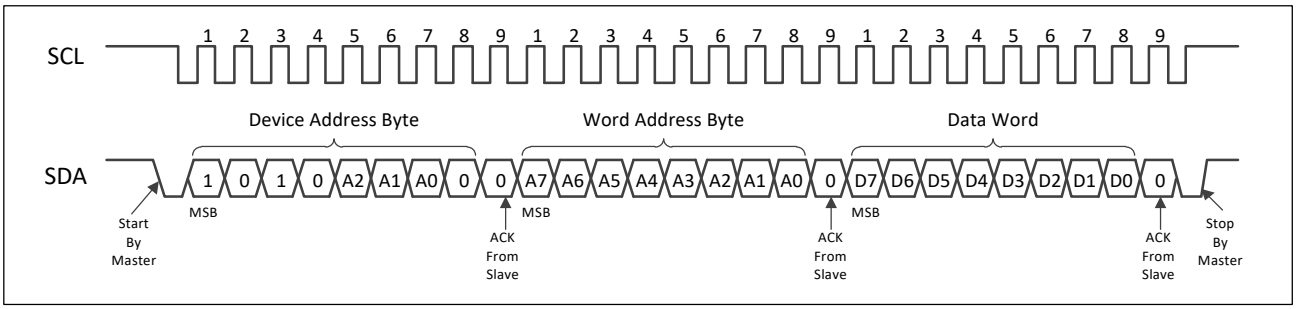
Table 5–2 Acknowledge Status When Writing Data or Defining Write Protection

Block Status	Instruction	ACK	Word Address	ACK	Data Word	ACK	Write Cycle
Write Protected	SWPn	NACK	Don't Care	NACK	Don't Care	NACK	No
	CWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write	ACK	Word Address	ACK	Data	NACK	No
Not Protected	SWPn	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	CWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write	ACK	Word Address	ACK	Data	ACK	Yes

5.3.1 Byte Write

For a Byte Write operation, the Master sends a Start condition followed by the device type identifier of '1010', the device address bits and the R/$\overline{W}$ select bit set to Logic 0. The WB34C04 responds with an ACK during the ninth clock cycle. Then the next byte transmitted by the Master is the 8-bit word address of the byte location to be written into the Serial EEPROM. After receiving an ACK from the WB34C04, the Master transmits the data word to be programmed followed by an ACK from the WB34C04. The Master ends the Write sequence with a Stop condition during the 10th clock cycle (see **Figure 5–6**) to initiate the internally self-timed write cycle. A Stop condition issued during any other clock cycle during the Write operation will not trigger the internal write cycle.
Once the write cycle begins, the preloaded data word will be programmed in the amount of time not to exceed the t_{WR} specification. During the time, the Master should wait a fixed time by the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented. All inputs are ignored by the device during the write cycle and the device will not respond until the write cycle is complete (see **Figure 5–8**). The Serial EEPROM will increment its internal address counter each time a byte is written.

Figure 5–6 Byte Write

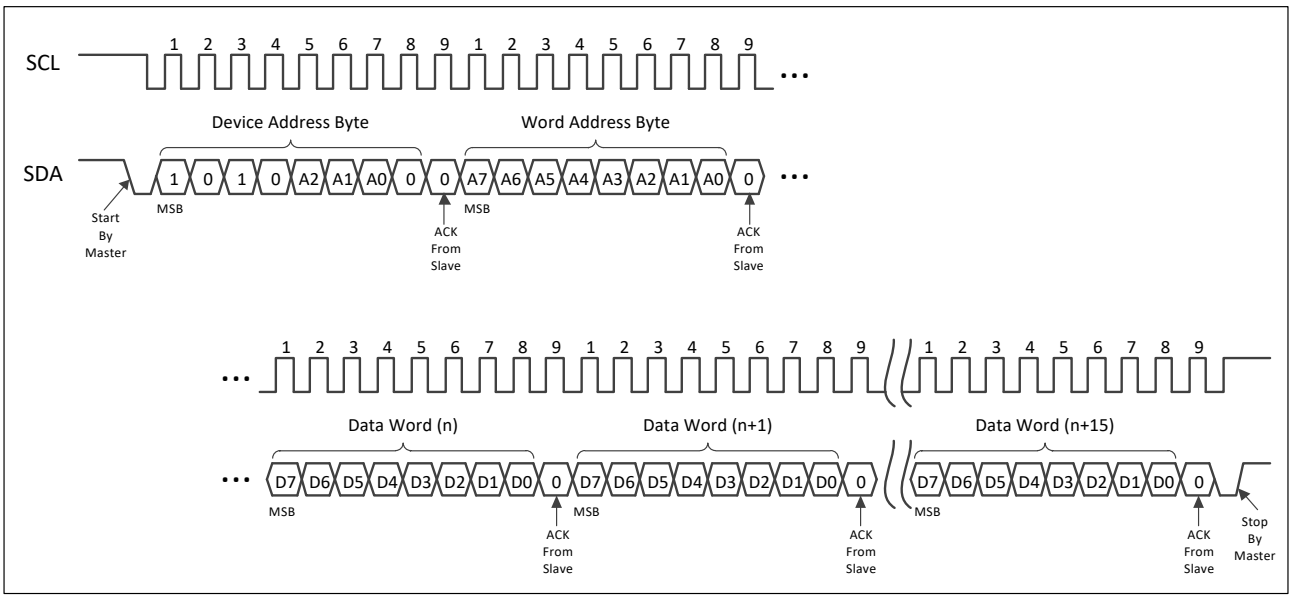


5.3.2 Page Write

The 4-Kbit Serial EEPROM is capable of writing up to 16 data bytes at a time by executing the Page Write protocol sequence. A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the device has acknowledged to the first data word, the Master can transmit up to fifteen more data words. The device will respond with an ACK after each data word is received (see **Figure 5–7**). After the device acknowledges to the last data word, the Master should terminate the Page Write sequence with a Stop condition to start the internal write cycle. A Stop condition issued at any other clock cycle will not initiate the internally self-timed write cycle and the Write sequence will have to be repeated again. Once the write cycle begins, the data words should be programmed in the amount of time not exceeding the t_{WR} specification (see **Figure 5–8**). During this time, the Master should wait a fixed time by the specified t_{WR} parameter, or for time sensitive applications, an ACK polling routine can be implemented.

The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, then the following data word is placed at the beginning of the same page. If more than sixteen data words are transmitted to the device, the data word address will roll-over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

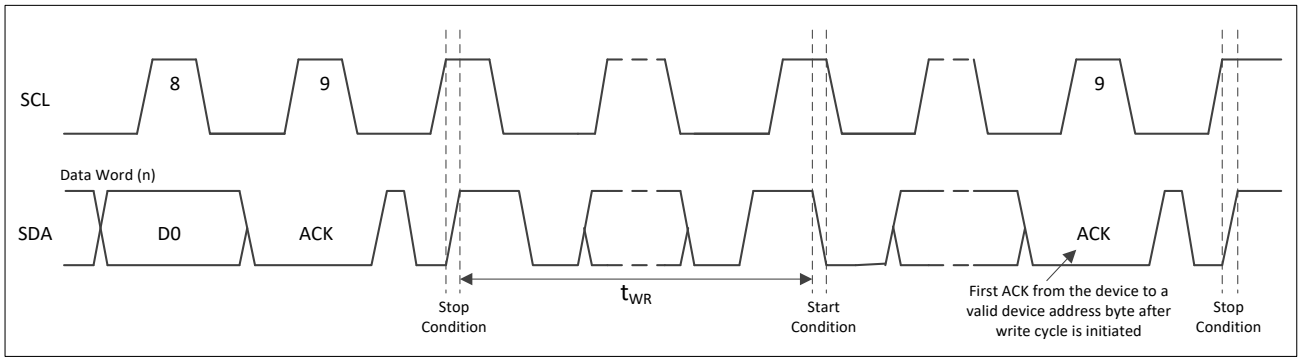
Figure 5–7 Page Write



5.3.3 Write Cycle Timing

The length of the self-timed write cycle, or t_{WR}, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the WB34C04 that it subsequently responds with an ACK (see **Figure 5–8**).

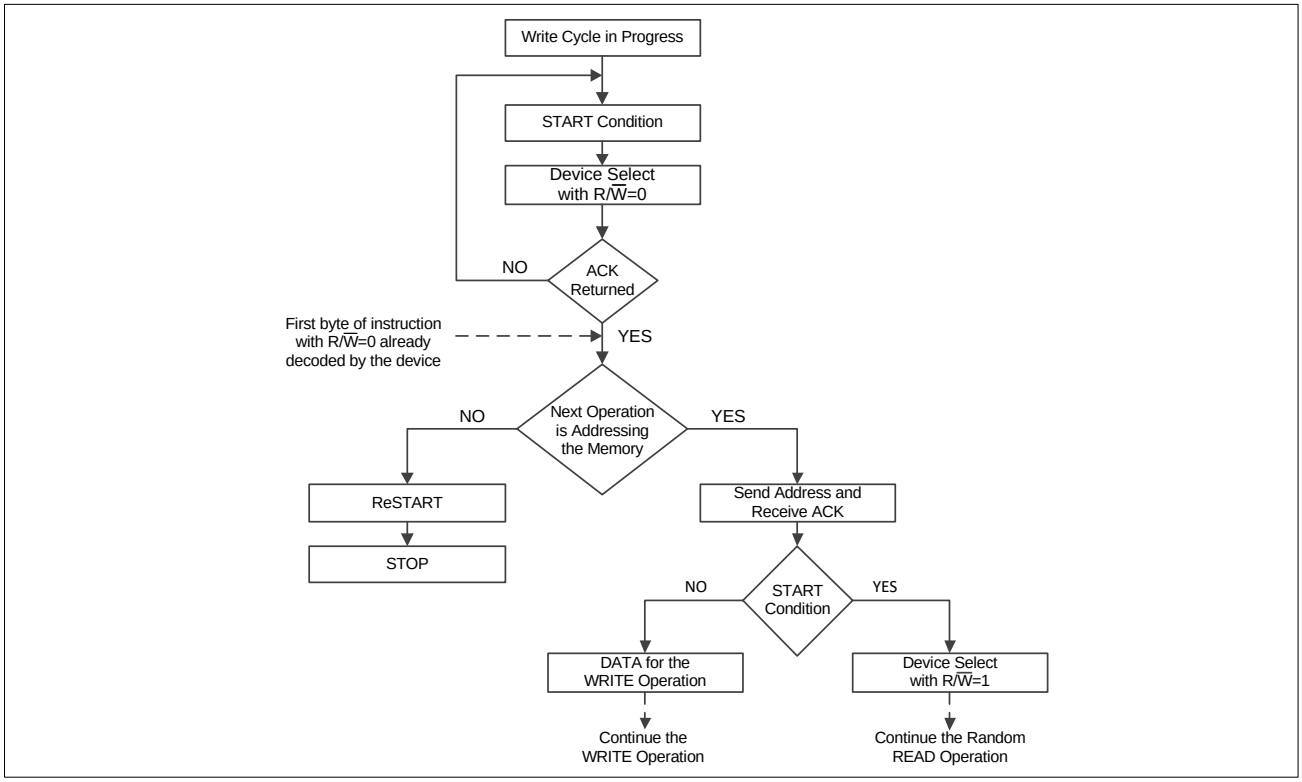
Figure 5–8 Write Cycle Timing



5.3.4 Acknowledge (ACK) Polling

An ACK polling routine can be implemented to optimize time sensitive applications that would not prefer to wait the fixed maximum write cycle time but would prefer to know immediately when the Serial EEPROM write cycle has completed to start a subsequent operation. Once the internally self-timed write cycle has started, the device inputs are disabled and ACK polling can be initiated. An ACK polling routine involves sending a valid Start condition followed by the device address byte. While the write cycle is in progress, the device will not respond with an ACK, indicating the device is busy writing data. Once completed, the device returns an ACK and the next device operation can be started (see **Figure 5–9**).

Figure 5–9 Acknowledge Polling Flow Chart



6 Write Protection

The WB34C04 has three software commands for setting, clearing, or checking the write protection:

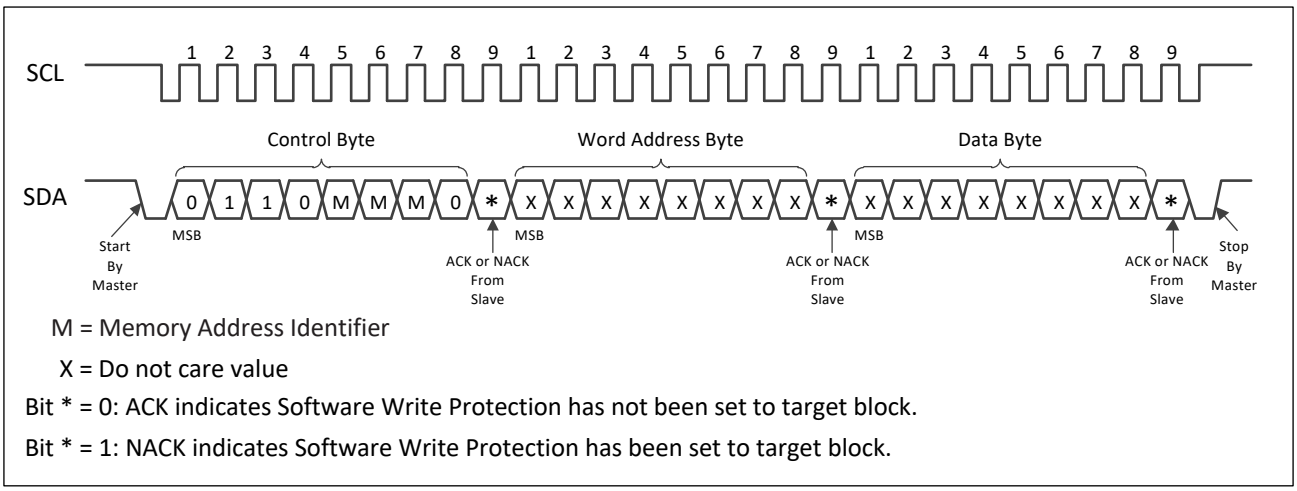
- SWPn: Set Write Protection for Block n
- CWP: Clear Write Protection for all blocks to an unprotected state
- RPSn: Read the Protection Status of Block n

The Software Write Protection feature allows the ability of selective write protection data stored in each of the four independent 128-byte blocks.

6.1 Set Write Protection

Setting the Write Protection is enabled by sending the Set Write Protection (SWPn) command to the target Block n. The SWPn sequence requires the Master to send a control byte of '0110MMM0' (where 'M' represents the memory address identifier for the block to be write-protected, see **Table 6–1**) with the R/$\overline{W}$ bit set to Logic 0. If the target block has not been write-protected, the WB34C04 responds with an ACK to the control byte. If Software Write Protection has been already set to the target block, the WB34C04 responds with a NACK (see **Table 5–2**). Then the Master transmits a word address byte and a data byte with Don't Care values followed by the WB34C04 responds to each of the word address byte and the data byte with an ACK or a NACK corresponding to the response on the control byte. To end the SWPn sequence, the Master sends a Stop condition (see **Figure 6–1**). Be sure that the SA0 pin is connected to V_{HV} for the duration of the SWPn sequence. If the SA0 pin is detected not to be connected to V_{HV}, none of the control byte, word address byte and data byte will be acknowledged by the WB34C04.

Figure 6–1 Set Write Protection



6.2 Clear Write Protection

The Write Protection status on all blocks can be reversed by transmitting the Clear Write Protection (CWP) command. The CWP sequence requires the Master to send a Start condition followed by sending a control byte of '01100110' with the R/$\overline{W}$ select bit set to Logic 0. The WB34C04 should respond with an ACK. Then the Master transmits a word address byte and a data byte with Don't Care values followed by the WB34C04 responds with an ACK to each of the word address byte and the data byte. To end the CWP sequence, the Master sends a Stop condition (see **Figure 6–2**). Be sure that the SA0 pin is connected to V_{HV} for the duration of CWP command. If the SA0 pin is detected not to be connected to V_{HV}, none of the control byte, word address byte and data byte will be acknowledged by the WB34C04.

The SWPn acts on a single block only as specified in the SWPn command and can only be reversed by issuing the CWP command and will unprotect all blocks in one operation (see **Table 6–1**).

Example: If Block 0 and Block 3 are needed to be write-protected, two separate SWP0 and SWP3 commands should be required; however, only one CWP command is needed to clear the write protection status of both blocks.

Figure 6–2 Clear Write Protection

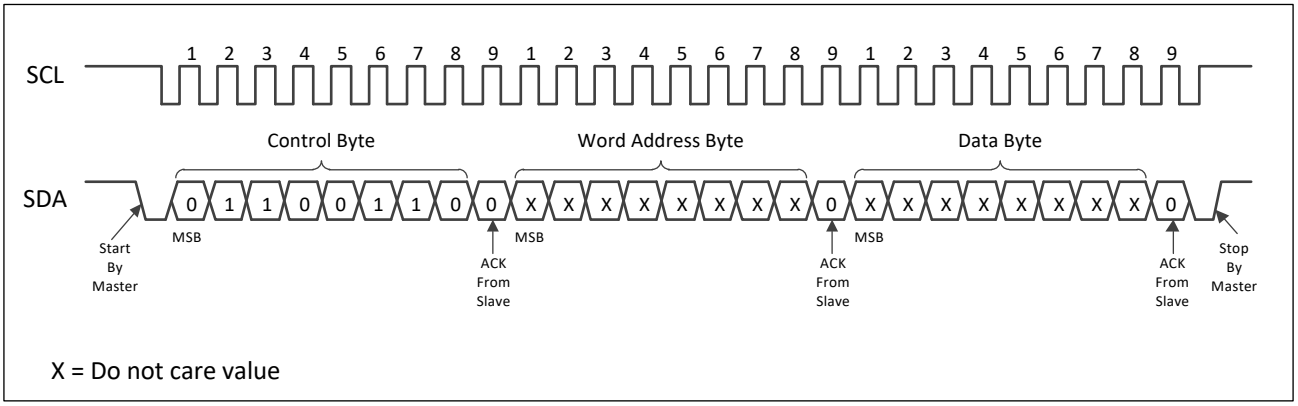


Table 6–1 SWPn, CWP and RPSn

Function	Pin			Control Byte							
				Device Type Identifier				Memory Address Identifier			R/$\overline{W}$
	SA2	SA1	SA0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Set Write Protection, Block 0	X[1]	X	V_{HV}[2]	0	1	1	0	0	0	1	0
Set Write Protection, Block 1	X	X						1	0	0	0
Set Write Protection, Block 2	X	X						1	0	1	0
Set Write Protection, Block 3	X	X						0	0	0	0
Clear All Write Protection	X	X						0	1	1	0
Read Protection Status, Block 0	X	X	0, 1 or V_{HV}	0	1	1	0	0	0	1	1
Read Protection Status, Block 1	X	X						1	0	0	1
Read Protection Status, Block 2	X	X						1	0	1	1
Read Protection Status, Block 3	X	X						0	0	0	1

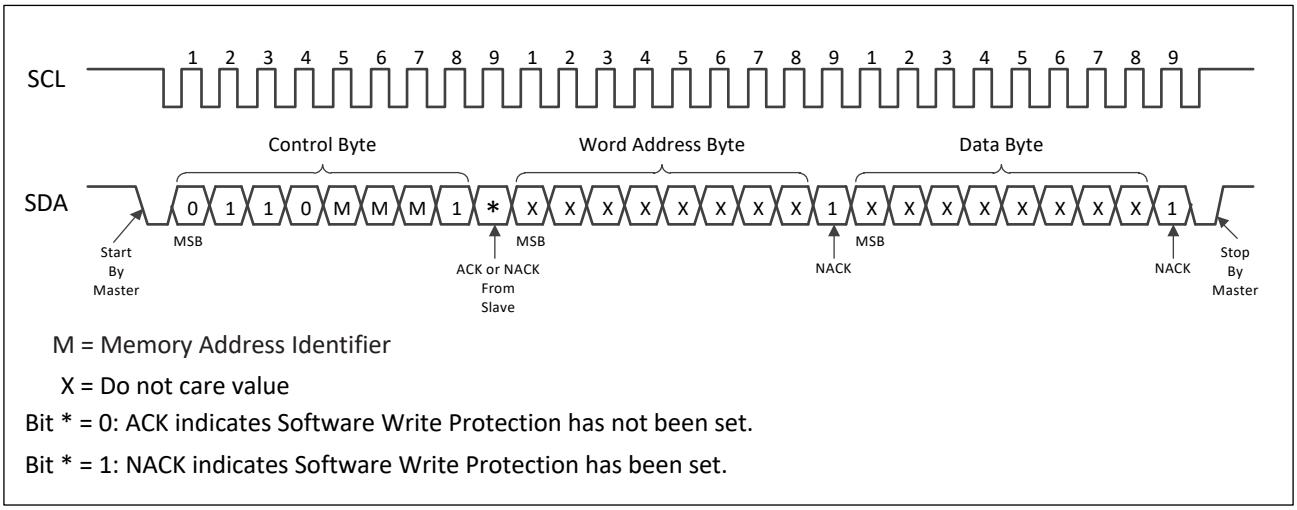
Notes: [1] X = Don't care but recommended to be hard-wired to V_{CC} or GND.

[2] See **Table 7–2** for V_{HV} value.

6.3 Read Protection Status

The Read Protection Status (RPSn) command allows the ability to check a block's write protection status. To find out if the Software Write Protection has been set to a specific Block n, the same procedure used to set the block's write protection can be utilized except that the R/$\overline{W}$ select bit is set to Logic 1, and the SA0 pin is not required to be connected to V_{HV} (see **Table 6–1**). The RPSn sequence requires the master to send a control byte of '0110MMM1' (where 'M' represents the memory address identifier for the block to be read) with the R/$\overline{W}$ bit set to Logic 1. If Software Write Protection has not been set to the target block, the WB34C04 responds to the control byte with an ACK. Alternately, If Software Write Protection has been set, the WB34C04 responds with a NACK. In either case, neither the word address byte nor the data byte with Don't Care values will be acknowledged (see **Figure 6–3**). The operation is completed by the Master creating a Stop condition.

Figure 6–3 Read Protection Status



7 Electrical Specifications

7.1 Absolute Maximum Ratings

Table 7–1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient temperature with power applied	-40 to +105	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{SA0}	Voltage on Pin SA0	-0.5 to +10	V
V_{IN}	Voltage on input Pins	-0.5 to +6.0	V

Note: Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 DC Characteristics

Operating range: T_A = -40°C to +105°C, V_{CC} = 1.7V to 3.6V (unless otherwise noted).

Table 7–2 DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{CC}	Supply Voltage		1.7	3.6	V
I_{CC1}	Supply Current (Read)	V_{CC}= 3.6V, Read at 1MHz	-	0.5	mA
I_{CC2}	Supply Current (Write)	V_{CC}= 3.6V, Write at 400kHz	-	1	mA
I_{SB}	Standby Current	V_{CC} = 3.6V, V_{IN} = V_{CC} or GND	-	1	μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	-	0.1	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	-	0.1	μA
V_{IL}	Input Low-Level Voltage (SDA, SCL)		-0.5	0.3*V_{CC}	V
V_{IH}	Input High-Level Voltage (SDA, SCL)		0.7*V_{CC}	V_{CC}+0.5	V
V_{OL1}	Low-Level Output Voltage	V_{CC}> 2V, I_{OL}= 3mA	-	0.4	V
V_{OL2}	Low-Level Output Voltage	V_{CC}≤2V, I_{OL}= 2mA	-	0.2*V_{CC}	V
I_{OL}	Low-Level Output Current	V_{OL} = 0.4V, F ≤ 400kHz	3.0	-	mA
		V_{OL} = 0.6V, F ≤ 400kHz	6.0	-	mA
V_{HV}	SA0 Pin High Voltage	V_{HV} – V_{CC} ≥ 4.8V	7	10	V

7.3 AC Characteristics

Operating range: T_A = -40°C to +105°C, V_{CC} = 1.7V to 3.6V, C_L = 100pF (unless otherwise noted).

Measurement conditions: Input rise and fall time ≤ 50ns

Input pulse voltages: 0.2*V_{CC} to 0.8*V_{CC}

Input and output timing reference voltages: 0.3*V_{CC} to 0.7*V_{CC}

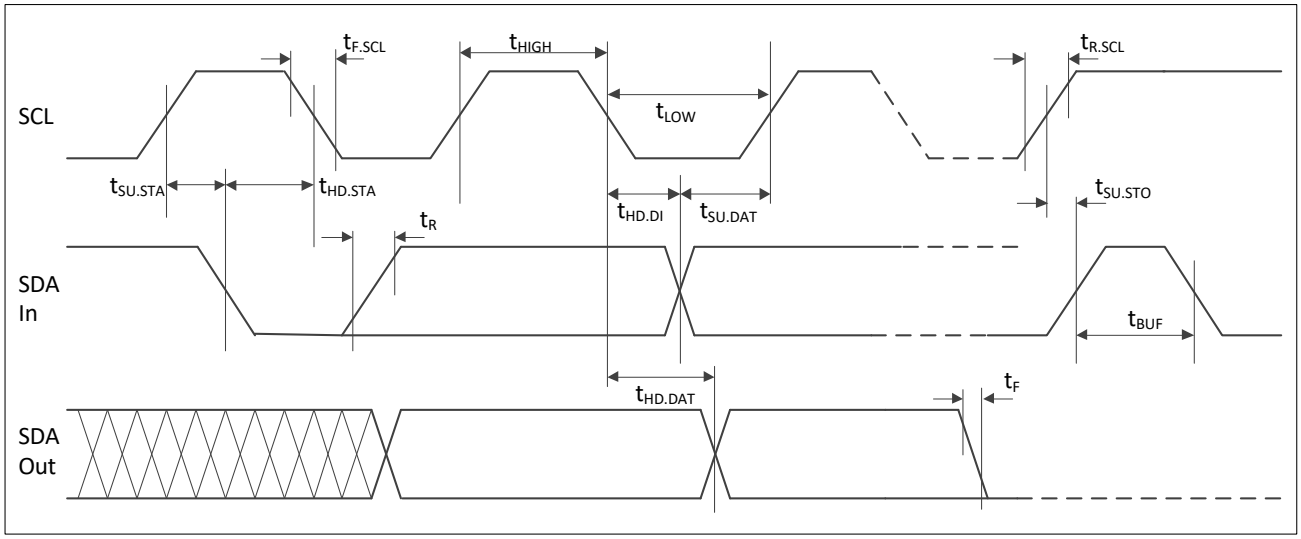
Table 7–3 AC Characteristics

Symbol	Parameter	V_{CC}<2.2V		V_{CC}>=2.2V				Unit
		100kHz		400kHz		1000kHz		
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL	10[2]	100	10[2]	400	10[2]	1,000	kHz
t_{LOW}	Clock Pulse Width Low	4,700	-	1,300	-	500	-	ns
t_{HIGH}	Clock Pulse Width High	4,000	-	600	-	260	-	ns
t_I	Noise Suppression Time	-	50	-	50		50	ns
t_{BUF}[1]	Time the bus must be free before a new transmission can start	4,700	-	1,300	-	500	-	ns
$t_{HD.STA}$	Start Hold Time	4,000	-	600	-	260	-	ns
$t_{SU.STA}$	Start Setup Time	4,700	-	600	-	260	-	ns
$t_{HD.DI}$	Data In Hold Time	0.0	-	0.0	-	0.0	-	ns
$t_{SU.DAT}$	Data In Set-up Time	250	-	100	-	50	-	ns
t_R[1]	SDA Rise Time	-	1,000	-	300	-	120	ns
t_F[1]	SDA(Out) Fall Time	-	300	-	300	-	120	ns
$t_{SU.STO}$	Stop Setup Time	4,000	-	600	-	260	-	ns
$t_{HD.DAT}$	Data Out Hold Time	200	3,450	200	900	0	350	ns
t_{WR}	Write Cycle Time	-	3	-	3	-	3	ms
t_{OUT}	Timeout Time	25	35	25	35	25	35	ms

Notes: [1] This parameter is ensured by characterization only.

[2] The minimum frequency is specified at 10kHz to avoid activating the timeout feature.

Figure 7–1 Bus Timing



7.4 Capacitance

Operating range for pin capacitance: T_A = +25°C, f_C = 1MHz, V_{CC} = 1.7V to 3.6V.

Table 7–4 Pin Capacitance

Symbol	Parameter[1]	Max	Unit	Test Condition
$C_{I/O}$	Input/output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SA0, SA1, SA2, SCL)	6	pF	V_{IN} = 0V

Note: [1] These parameters are ensured by characterization only.

7.5 Reliability

Table 7–5 Reliability Performance

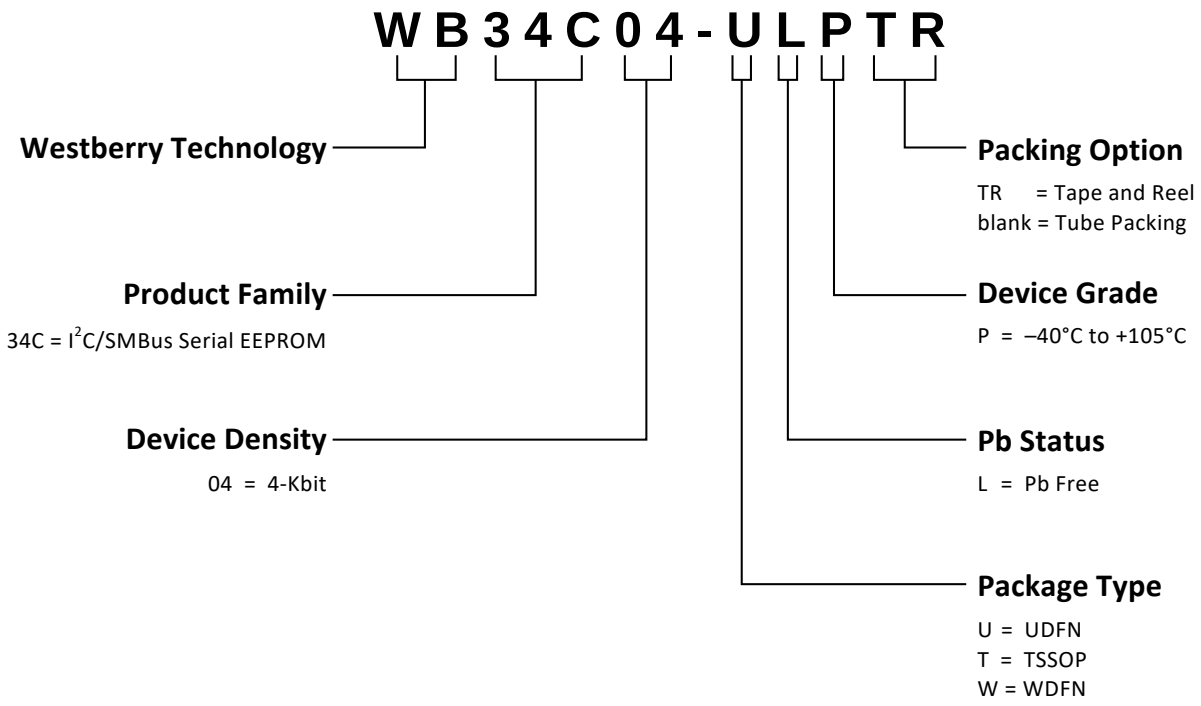
Symbol	Parameter	Min	Unit	Test Condition
N_W	Write Cycle Endurance	$5x10^6$	cycle	T_A = +25°C, Page Mode
D_R	Data Retention	100	year	T_A = +25°C

8 Initial Delivery State

The WB34C04 EEPROM is delivered with all bits in the memory array set to ‘1’ (each byte contains FFh).

9 Ordering Information

Table 9–1 Ordering information scheme

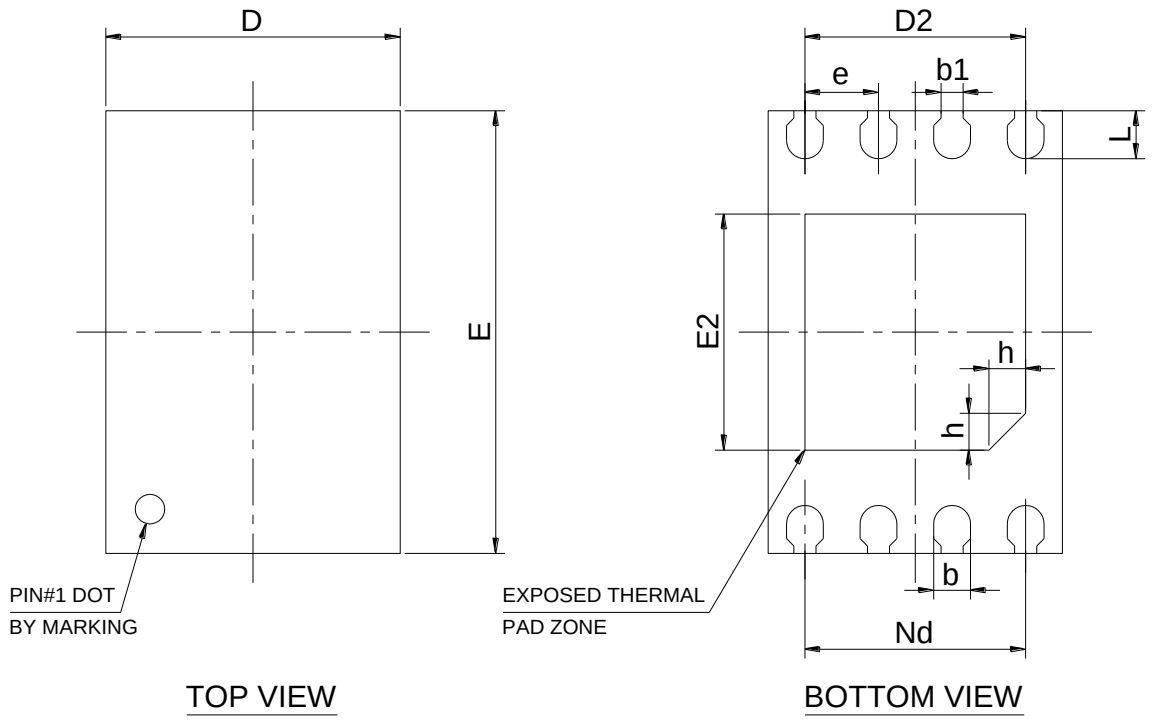


Part Number	Package	Delivery Information	Temperature Range
WB34C04-ULPTR	2.0 x 3.0mm UDFN	Tape and Reel, 3000 units per Reel	-40°C to +105°C
WB34C04-TLPTR	3.0 x 4.4mm TSSOP	Tape and Reel, 5000 units per Reel	-40°C to +105°C
WB34C04-WLPTR	2.0 x 3.0mm WDFN	Tape and Reel, 3000 units per Reel	-40°C to +105°C

10 Package Information

10.1 UDFN Package Information

Figure 10–1 8-lead 2.0 x 3.0 x 0.55 mm UDFN Package Outline



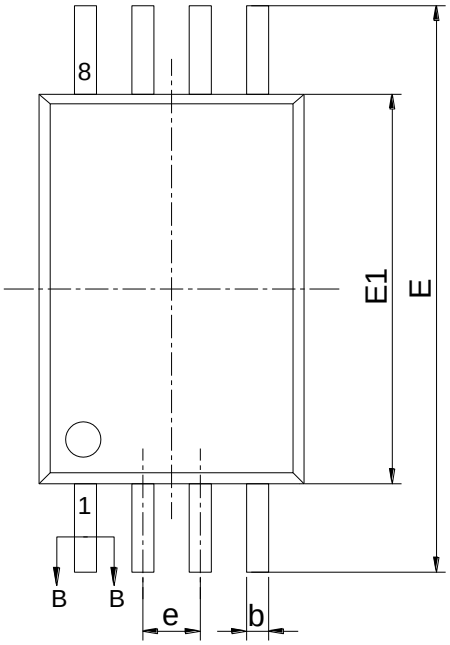
SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1	0.16REF		
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.30	0.40	0.50
h	0.20	0.25	0.30

Note:

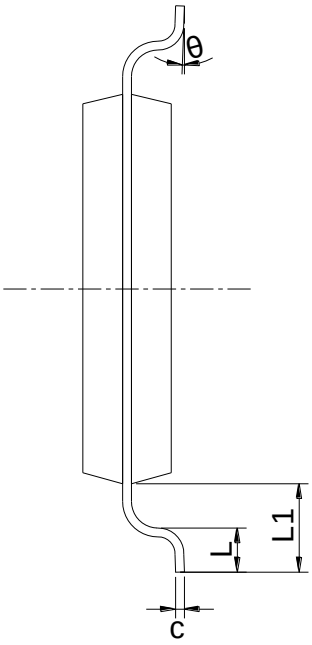
1. Controlling dimension is mm.
2. Drawing is not to scale.
3. Refer to JEDEC standard MO-229.
4. Default thickness marked by symbol A is 0.55mm (NOM), 0.50mm (NOM) is an alternative if needed.

10.2 TSSOP Package Information

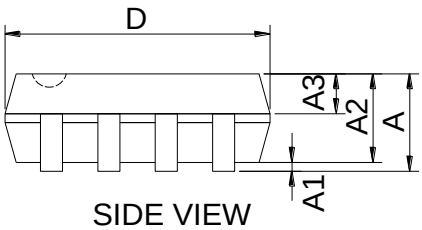
Figure 10–2 8-pad 3.0 x 4.4mm TSSOP Package Outline



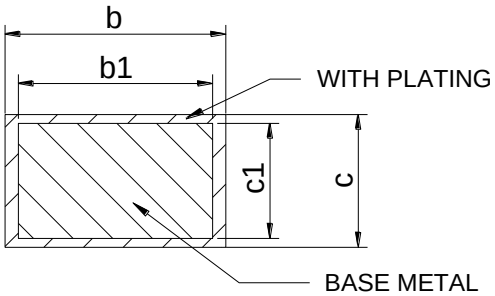
TOP VIEW



END VIEW



SIDE VIEW



SECTION B-B

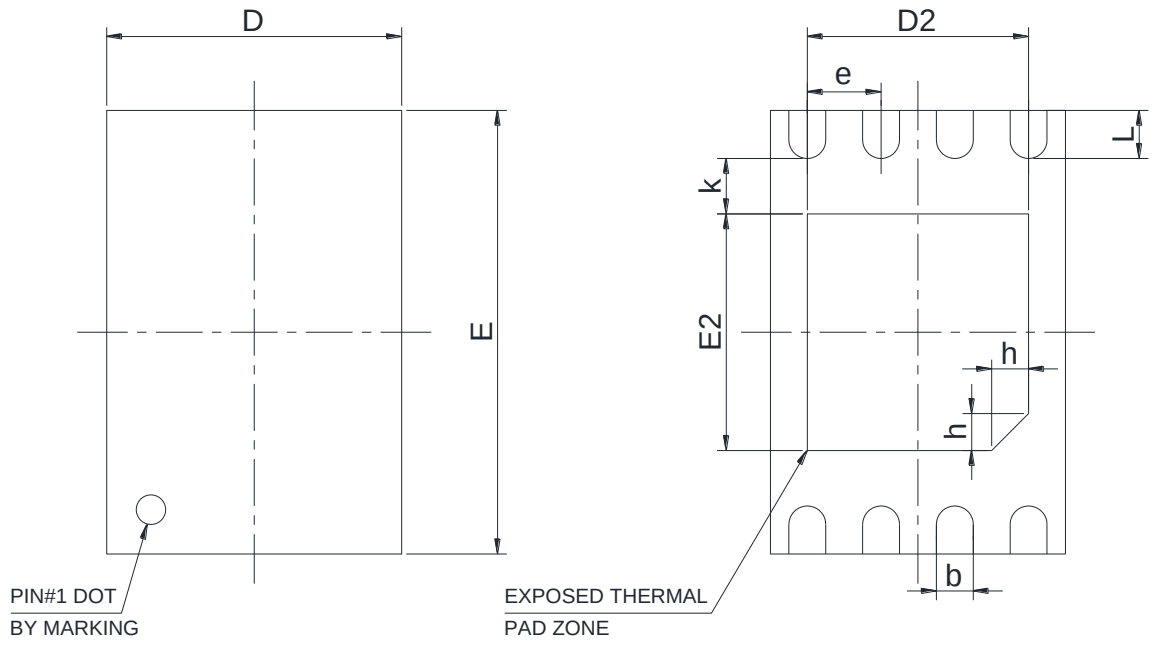
Note:

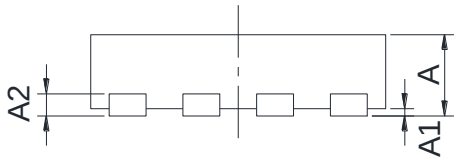
1. Controlling dimension is mm.
2. Drawing is not to scale.
3. Refer to JEDEC standard MO-153.

SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.50	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°

10.3 WDFN Package Information

Figure 10–3 8-lead 2.0 x 3.0 x 0.75 mm WDFN Package Outline





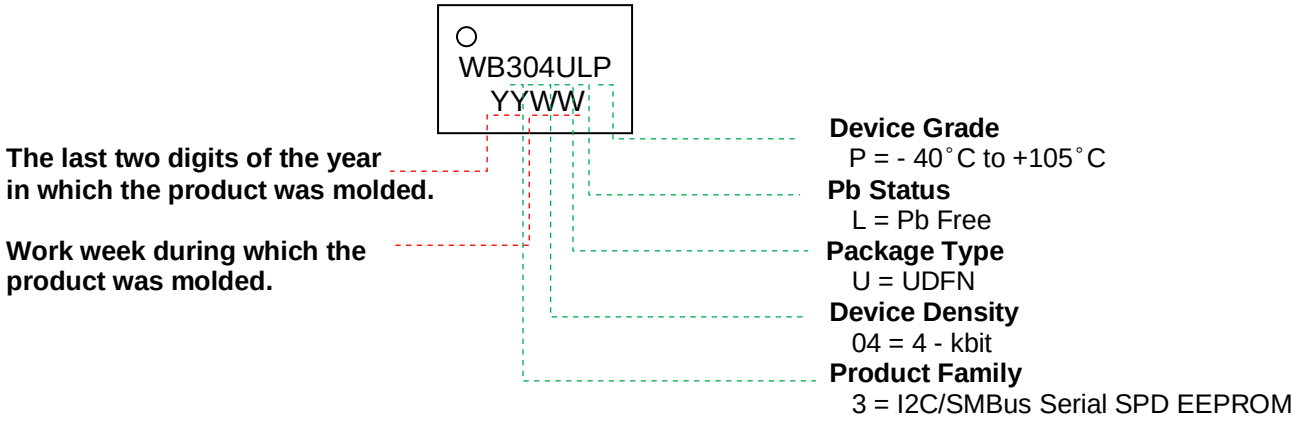
Note:

1. Controlling dimension is mm.
2. Drawing is not to scale.

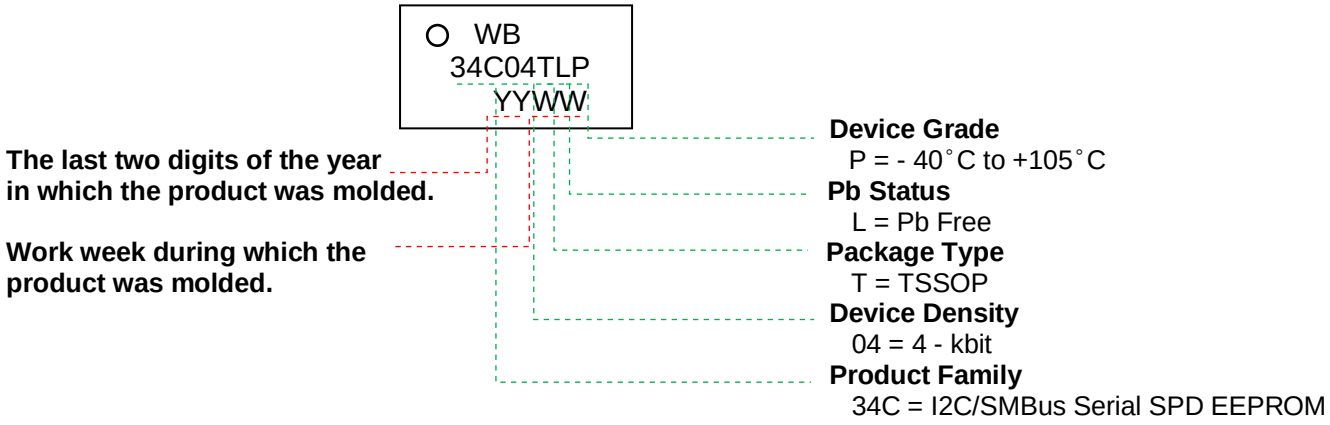
SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2		0.203 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
e		0.50 BSC	
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.35	0.40	0.45
h	0.20	0.25	0.30
k	0.25	0.30	0.35

11 Park Marking Scheme

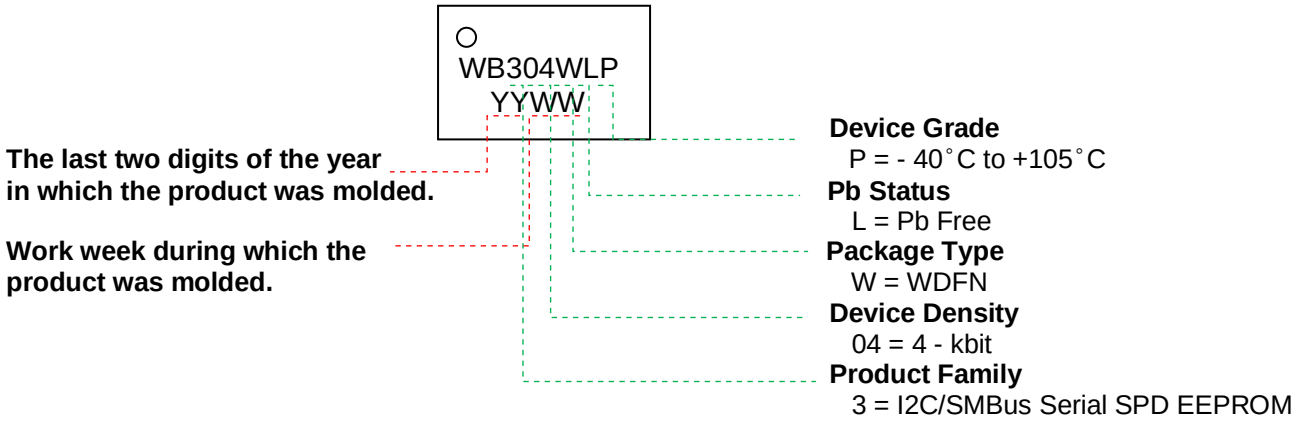
11.1 UDFN(2.0 x 3.0mm)



11.2 TSSOP(3.0 x 4.4mm)



11.3 WDFN(2.0 x 3.0mm)



12 Revision History

Revision	Date	Comments
Rev.1.0	Dec. 2018	Initial version release
Rev.1.1	Jun. 2019	Document reformatted Updated: — *Features* — Write Cycle Endurance value in *Table 7–5*
Rev.1.2	Oct.2020	Document reformatted Updated: — Park Marking Scheme