WB34TS04

Temperature Sensor with 4-Kbit SPD EEPROM

DATASHEET

Features

- Temperature Sensor with Integrated 4-Kbit SPD EEPROM
- Fully Compliant with JEDEC TSE2004av Specification
- Supply Voltage: 1.7V to 3.6V
- 2-wire Serial Interface I^2C/SMBus Compatible
  - — Up to 1 MHz Transfer Rate (I^2C Fast Mode+) Supported
  - — Bus Timeout Supported
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Operating Temperature Range: -40°C to +125°C
- Green Packaging Option (RoHS Compliant, Pb/Halogen-free)
  - — 8-Lead UDFN

Temperature Sensor

- Temperature Sensor Accuracy
  - — ± 0.5°C (typical) from +75°C to +95°C
  - — ± 1°C (typical) from +40°C to +125°C
  - — ± 2°C (typical) from -40°C to +125°C
- Temperature Sensor Resolution
  - — 10-bit Analog-to-digital Converter with 0.25°C/LSB Resolution (default)
  - — Programmable 9-12 Bits
- ADC Conversion Time: 125ms (maximum)
- Programmable Temperature Hysteresis Threshold: 0, 1.5, 3 and 6.0°C
- Low Operating Current
  - — Temperature Sensor Active (EEPROM Standby): 0.2mA (maximum)
  - — Temperature Sensor Shutdown (EEPROM Standby): 5μA (maximum)

SPD EEPROM

- Functionality Identical to WB34C04 SPD EEPROM
- Software Data Protection on all Four 128-byte Blocks
- Byte and Page Write Mode
  - — Page Size up to 16 Bytes
- Self-timed Write Cycle: 3ms (maximum)
- Operating Temperature range: -40°C to +125°C
- High Reliability
  - — Endurance: 2,000,000 Write Cycles
  - — Data Retention: 200 Years
- Low Operating Current
  - — SPD EEPROM Write Current: 1mA (maximum)
  - — SPD EEPROM Read Current: 0.5mA (maximum)

Table of Contents

1 Description

The WB34TS04 is a temperature sensor product with embedded 4-Kbit Serial Presence Detect (SPD) EEPROM, which is fully compatible to industrial standard I^2C/SMBus interface and compliant to the JEDEC TSE2004av specification. The EEPROM memory is organized as two Pages of 256 bytes each, or 512 bytes of total memory. Each page is comprised of two 128-byte blocks. The device is able to selectively lock the data in any or all of the four 128-byte blocks. This product is designed for memory module applications in most PC and server platforms, as well as other related applications. All the information concerning the DRAM Dual Inline Memory Modules (DIMMs) configuration content (such as its access speed, its size, and its organization) can be kept write protected in one or more of the blocks of memory.

The WB34TS04 operates in a supply voltage range of 1.7V to 3.6V and is offered in 8-Pin Ultra-thin DFN package, 2mm x 3mm x 0.6mm (maximum), which is lead/halogen free, RoHS compliant, providing space as well as cost saving for DIMM manufactures.

The embedded 4-Kbit SPD EEPROM is protocol compatible with previous generation 2-Kbit device. The page selection method allows commands used with legacy device to applied to the lower or upper pages of the EEPROM/Temperature Sensor. In this way, the WB34TS04 may be used in legacy applications without software changes. Individually locking a 128-byte block of the EEPROM may be accomplished using a Software Write Protection mechanism in conjunction with a high input voltage V_{HV} on input SA0. By sending the device a specific I^2C Bus sequence, each block may be protected from writes until write protection is electrically reversed using a separate I^2C Bus sequence which also requires V_{HV} on input SA0. Write protection for all four blocks is cleared simultaneously, and write protection may be re-asserted after being cleared. The operating ambient temperature range of the EEPROM is from -40°C to +125°C.

The temperature sensor monitors the ambient temperature range from -40°C to 125°C. The temperature sensor includes a high precision band gap type temperature sensor, a sigma-delta analog to digital converter (ADC) and a serial interface compatible to industrial standard I^2C/SMBus. The ADC default resolution is set at 10-bit (0.25°C/LSB). The accuracy over various temperature ranges is:

± 0.5°C (typical) for an active range from +75°C to +95°C

± 1°C (typical) for a monitor range from +40°C to +125°C

± 2°C (typical) for a temperature range from -40°C to 125°C

The temperature sensor can be set in power-saving Shutdown mode with a low current of 2μA (typical) with SPD EEPROM in Standby mode.

The temperature sensor component has user-programmable registers that are used to configure both the temperature sensor performance and response to over-temperature conditions. The device contains programmable high, low and critical temperature limits. The $\overline{\text{EVENT}}$ pin can be configured as active high or active low and can be configured to operate as an Interrupt or as a Comparator output.

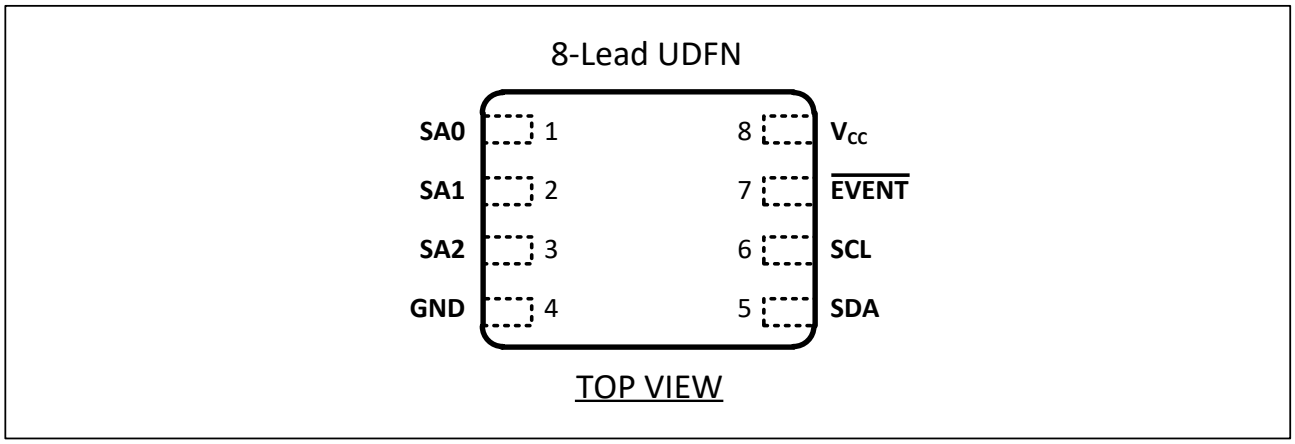
2 Pin Configuration

Table 2–1 Pin Descriptions

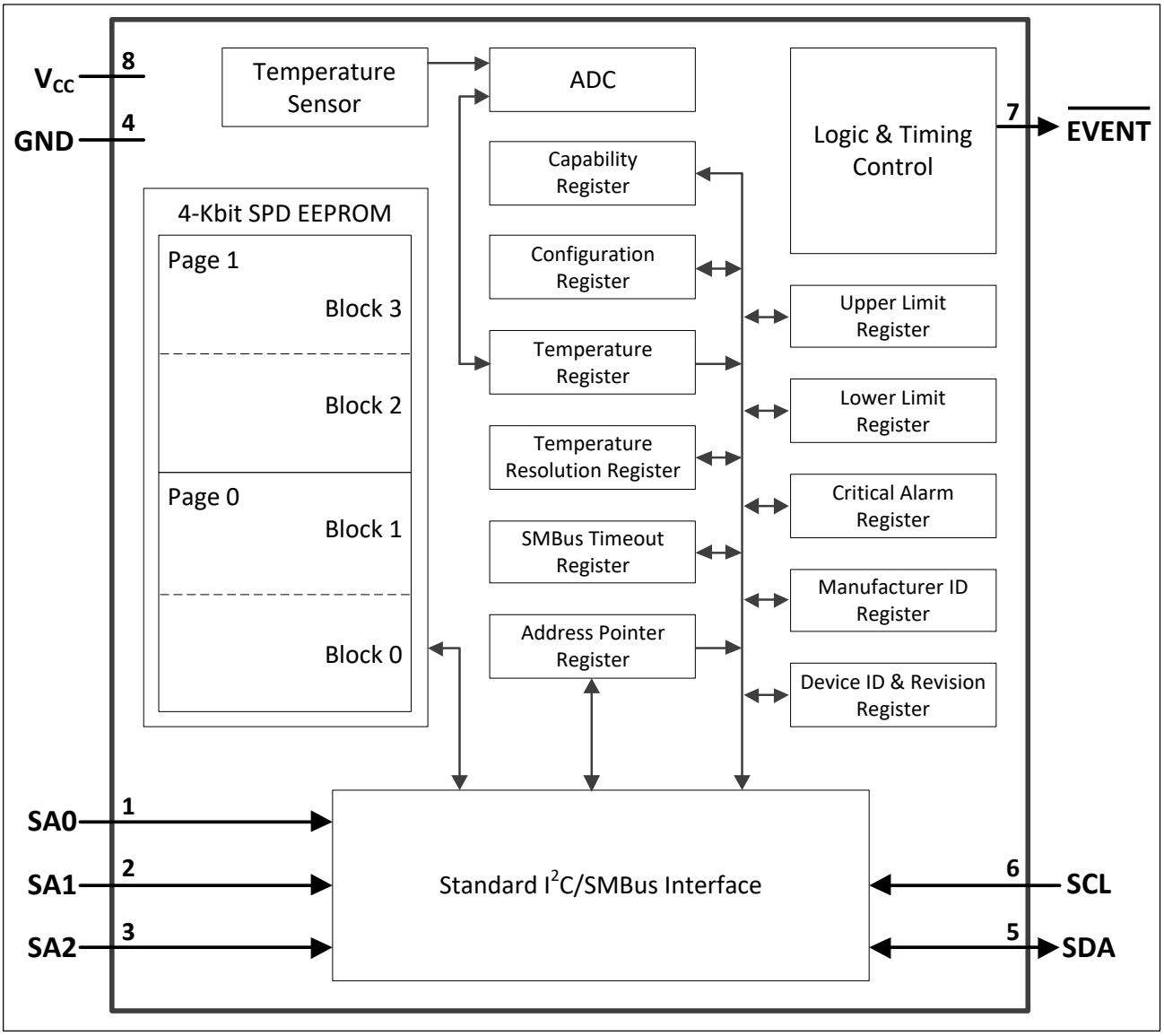
Symbol	Type	Name and Function
SA0 SA1 SA2	Input	**Device Address Inputs:** The SA0, SA1, and SA2 pins are used to select the device address and correspond to the three Least Significant Bits of the I^2C/SMBus seven-bit slave address. These pins can be directly connected to V_{CC} or GND in any combination, allowing up to eight devices on the same bus. The SA0 pin is also used to detect the V_{HV} voltage, when decoding a SWPn or CWP instruction. See **Table 7–3** for decode details.
SDA	Input/Output	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device.
SCL	Input	**Serial Clock:** The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL.
V_{CC}	Power	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.
GND	Power	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.
$\overline{\text{EVENT}}$	Output	**$\overline{\text{EVENT}}$:** The $\overline{\text{EVENT}}$ pin is an open-drain output pin and is active-low. A pull-up resistor must be connected to this pin. It has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt Mode, Comparator Mode and TCRIT Only Mode. See **Section 6.5.1** for details.

Note: Thermal sensing devices also have a heat paddle, typically connected to the application ground plane.

Figure 2–1 Pin Configuration



3 Functional Block Diagram



4 Device Communication

The WB34TS04 operates as a slave device and utilizes a 2-wire serial interface to communicate with the Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). Data is always latched into the WB34TS04 on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL pin and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

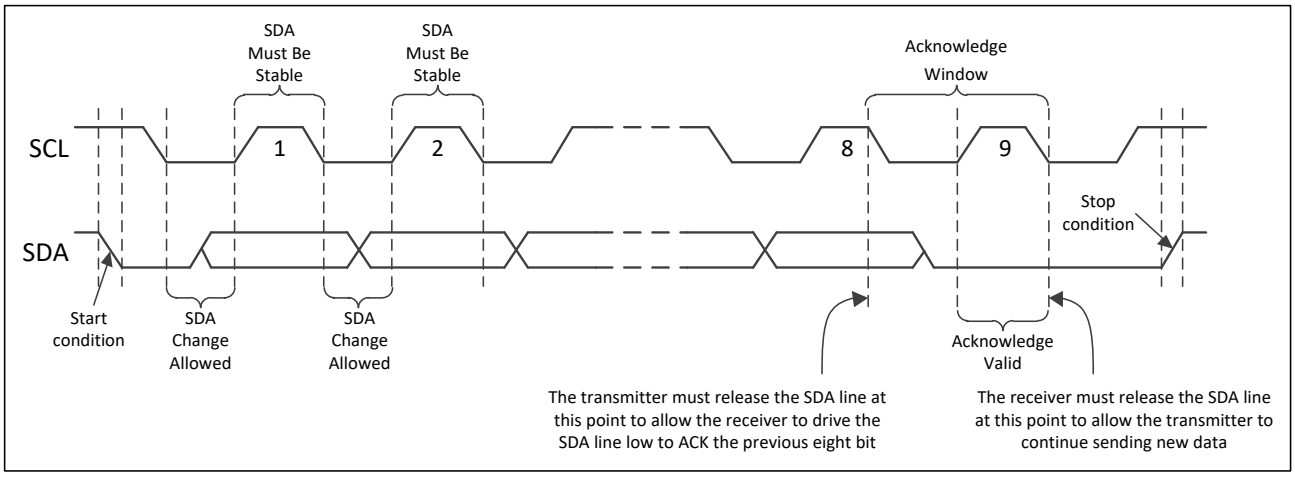
All command and data information is transferred with the Most Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after eight bits of data has been transferred, the receiving device must respond with an acknowledge or a no-acknowledge response bit during a ninth clock cycle generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There is no unused clock cycle during any Read or Write operation, so there must not be any interruptions or breaks during the data stream.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

4.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in Logic 1 state. The Start condition must precede any command as the Master uses a Start condition to initiate any data transfer sequence (see **Figure 4–1**). The WB34TS04 will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given.

Figure 4–1 Start, Stop, and ACK



4.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in Logic 1 state (see **Figure 4–1**). A stop condition terminates communication between the WB34TS04 and the Master. A Stop condition at the end of a Write command triggers the EEPROM internal write cycle. Otherwise, the WB34TS04 subsequently returns to Standby mode after receiving a Stop condition.

4.3 Acknowledge (ACK)

After each byte of data is received, the WB34TS04 should acknowledge to the Master that it has received the data byte successfully. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the WB34TS04 must output Logic 0 as ACK for the entire clock cycle so that the SDA line must be stable in Logic 0 state during the entire high period of the clock cycle (see **Figure 4–1**).

When the WB34TS04 is transmitting data to the Master, the Master can indicate that it is done receiving data and end the operation by sending a NACK response to the WB34TS04 instead of an ACK response. This is accomplished by the Master outputting Logic 1 during the ACK/NACK clock cycle, at which point the WB34TS04 should release the SDA line so that the Master can then generate a Stop condition.

In addition, the WB34TS04 can use a NACK to respond to the Master instead of an ACK for certain invalid operation cases such as an attempt to Write to a Read-only register.

4.4 Device Reset and Initialization

The WB34TS04 incorporates an internal Power-On Reset (POR) circuit to prevent inadvertent operations during power-up. On a cold power-up, the device does not respond to any instructions until the supply voltage reaches the internal reset threshold voltage (V_{POR}). The supply voltage must rise continuously between V_{POR} and V_{CC}(Min) without any ring back to ensure a proper power-up (see **Figure 4–2**). Once the supply voltage passes V_{POR}, the device is reset. However, no protocol should be issued to the device until a valid and stable supply voltage is applied for the time specified by the t_{INIT} parameter. The supply voltage must remain stable and valid until the end of the protocol transmission, and for a Write instruction, until the end of the internal write cycle.

At power down (phase during which V_{CC} decreases continuously), as soon as V_{CC} drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands. On warm power cycling, V_{CC} must remain below V_{POFF} for T_{POFF}, and must meet cold power on reset timing when restoring power.

Parameters related to power-up conditions are listed in **Table 4–1**.

Figure 4–2 Power-up Timing

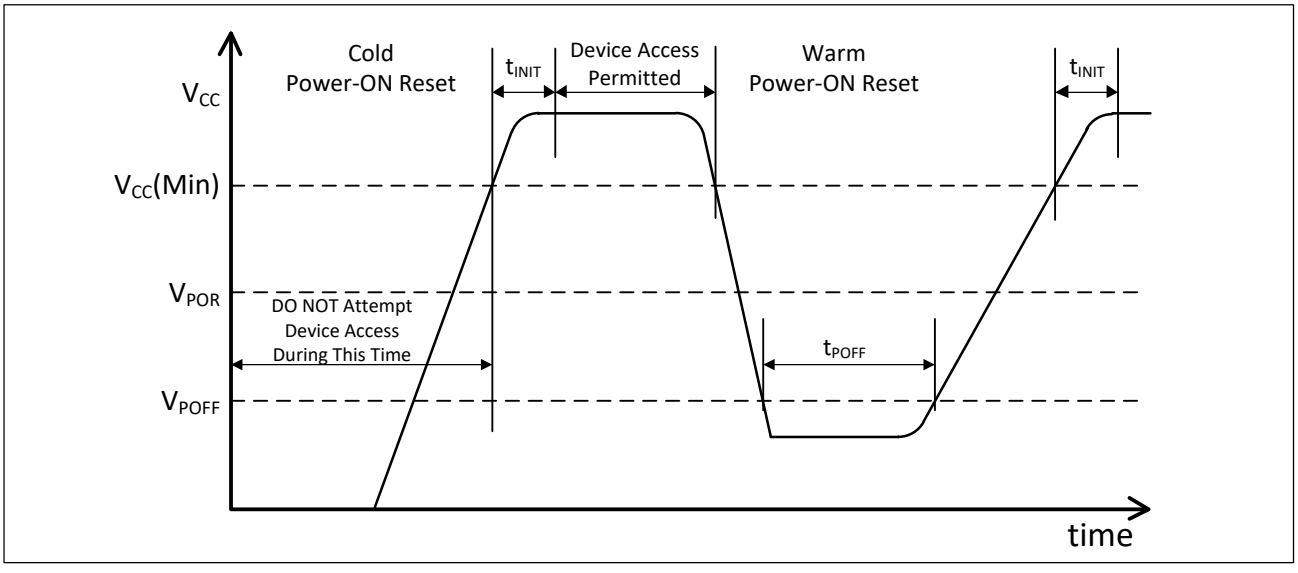


Table 4–1 Power-up Conditions

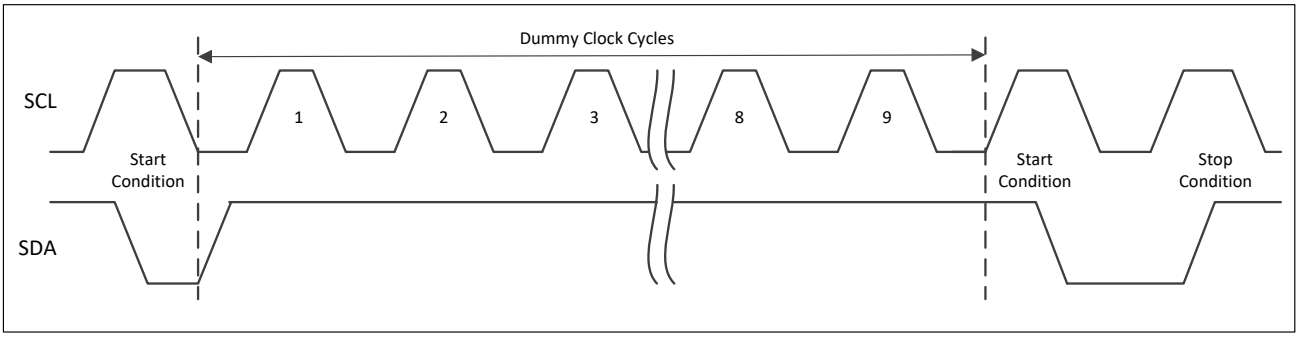
Symbol	Parameter	Min	Max	Unit
V_{POR}	Power-On Reset Threshold Voltage	1.6	-	V
V_{POFF}	Power-off Threshold for Warm Power-on Cycle	-	0.9	V
t_{INIT}	Time from Power-On to First Command	10.0	-	ms
t_{POFF}	Warm Power Cycle Off Time	1.0	-	ms

4.5 Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition.
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition (see **Figure 4–3**).

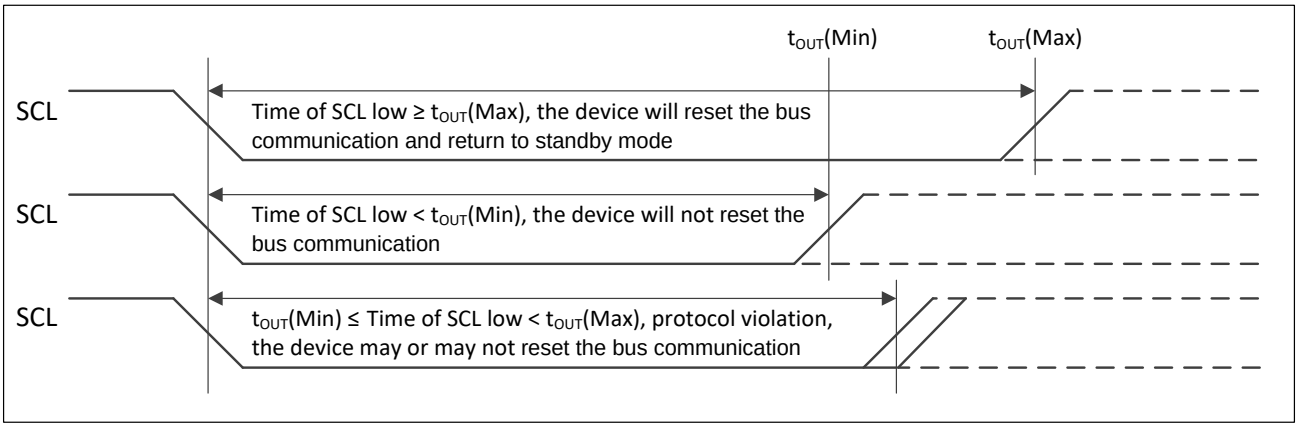
Figure 4–3 2-wire Software Reset



4.6 Timeout Function

The WB34TS04 supports the industry standard bus Timeout feature to prevent potential system bus lock-ups. The device resets the serial interface and returns to standby mode if the SCL pin is held low for more than the maximum Timeout t_{OUT}(Max) specification. If the SCL pin is held low for less than the minimum Timeout t_{OUT}(Min) specification, the device will not reset the serial interface (see **Figure 4–4**). This feature requires a minimum SCL clock speed of 10kHz to avoid any timeout issues.

Figure 4–4 Bus Timeout



5 Device Addressing

The WB34TS04 is designed to allow the temperature sensor and the SPD EEPROM to operate in parallel while executing valid command protocol. For example, when the temperature sensor is busy during a temperature conversion cycle, it is possible to perform any SPD EEPROM operation during this time.

The device requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with either the temperature sensor or the SPD EEPROM. The device address byte is comprised of a 4-bit device type identifier (DTI) followed by three device address bits (A2, A1, and A0) and a R/$\overline{W}$ bit and is clocked by the Master on the SDA pin with the most significant bit (bit 7) first (see **Table 5–1**).

The WB34TS04 will respond to three unique device type identifiers. The device type identifier of ‘1010’ is necessary to select the SPD EEPROM for Read or Write operation. The device type identifier of ‘0110’ is used to access the page address function which determines what the internal address counter is set to. The device type identifier of ‘0110’ is also used to access the Software Write Protection feature of the device. The device type identifier of ‘0011’ is used to access the temperature sensor registers for Read or Write operation.

The software device address bits (A2, A1 and A0) must match their corresponding hard-wired device address inputs (SA2, SA1 and SA0) (see **Table 5–2**), allowing up to eight devices on the bus at the same time. The eighth bit of the address byte is the R/$\overline{W}$ operation selection bit. A Read operation is selected if this bit is Logic 1, and a Write operation is selected if this bit is Logic 0. Upon a compare of the device address byte, the WB34TS04 will output an ACK or a NACK during the ninth clock cycle if the compare is true or not true. The device will return to the low-power Standby Mode after a NACK.

Table 5–1 WB34TS04 Device Address Byte

Function	Device Type Identifier				Device Address			Read/Write
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SPD EEPROM Read and Write Operations	1	0	1	0	A2	A1	A0	R/$\overline{W}$
SPD EEPROM Write Protection and Page Address Functions	0	1	1	0	A2	A1	A0	R/$\overline{W}$
Temperature Sensor Registers	0	0	1	1	A2	A1	A0	R/$\overline{W}$

Table 5–2 Device Address Combinations

Software Device Address Bits	Hard-wired Device Address Inputs		
A2, A1, A0	SA2	SA1	SA0
0 0 0	GND	GND	GND
0 0 1	GND	GND	V_{CC}
0 1 0	GND	V_{CC}	GND
0 1 1	GND	V_{CC}	V_{CC}
1 0 0	V_{CC}	GND	GND
1 0 1	V_{CC}	GND	V_{CC}
1 1 0	V_{CC}	V_{CC}	GND
1 1 1	V_{CC}	V_{CC}	V_{CC}

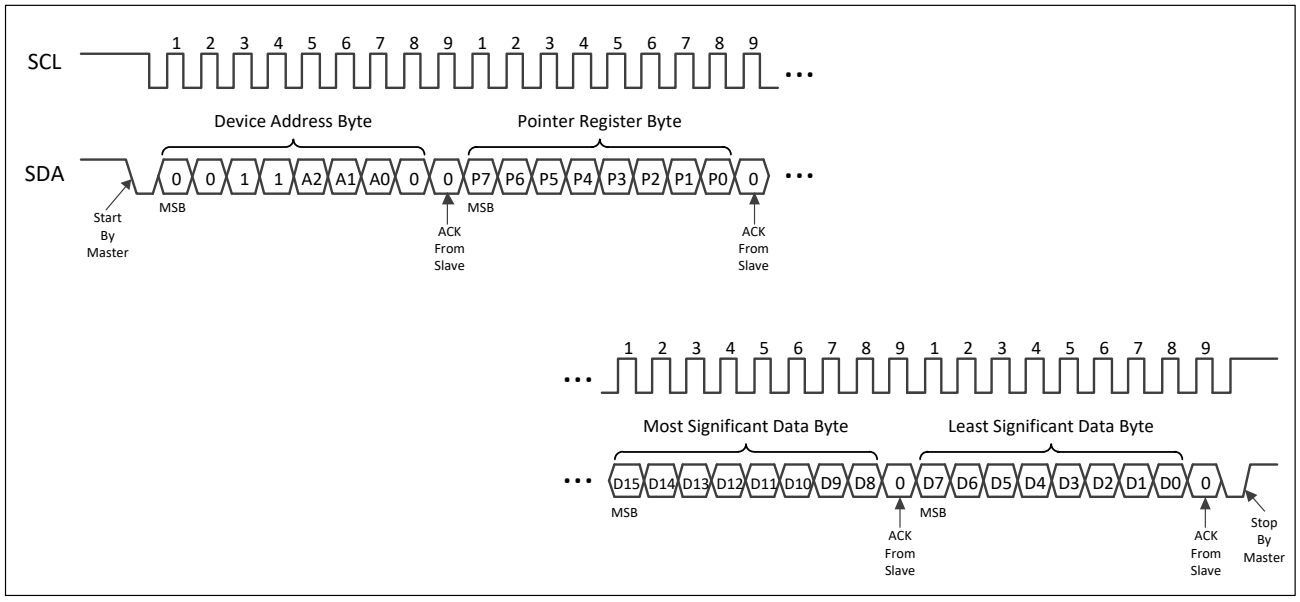
6 Temperature Sensor

The temperature sensor component consists of a Sigma-Delta analog-to-digital converter (ADC) with a band gap type temperature sensor and continuously monitors the ambient temperature and updates the temperature data register. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

6.1 Temperature Sensor Write Operation

Writing to the WB34TS04 Temperature Register Set is accomplished through a modified block write operation for two data bytes. To maintain I^2C Bus compatibility, the 16-bit register is accessed through a Pointer Register, requiring the write sequence to include an Address Pointer in addition to the Slave address, which indicates the storage location for the next two bytes received. **Figure 6–1** shows an entire write transaction on the bus.

Figure 6–1 Temperature Sensor Write Operation



6.2 Temperature Sensor Read Operation

Reading data from the temperature sensor may be accomplished in one of two ways:

1 If the location latched in the Pointer Register is correct (for normal operation it is expected the same address will be read repeatedly for temperature), the read sequence may consist of a Slave Address from the bus master followed by two bytes of data from the device; or

2 The pointer register is loaded with the correct register address, and the data is read. The preset pointer read is shown in **Figure 6–2**. If it is desired to read random address each cycle, the complete Pointer Write, Word Read sequence is shown in **Figure 6–3**.

The data byte has the most significant bit first. At the end of a read, this device can accept either ACK or NACK from the Master (NACK is typically used as a signal for the slave that the Master has read its last byte).

Figure 6–2 I²C Bus Preset Pointer Register Word Read

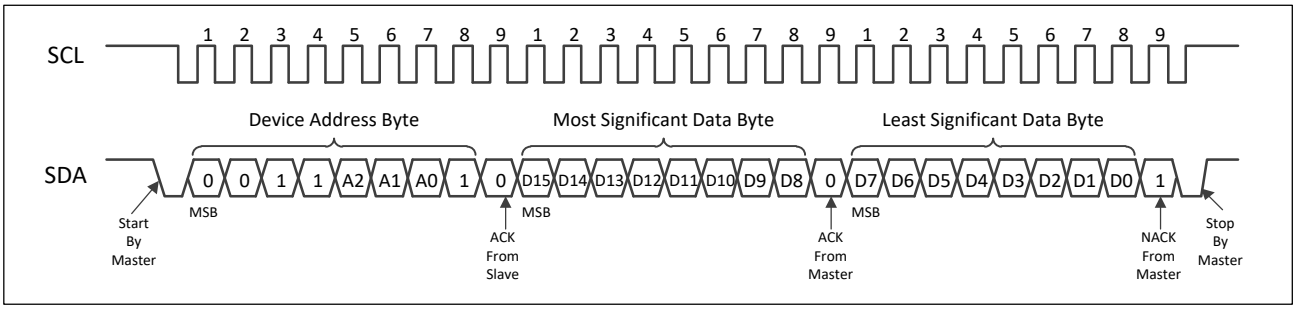
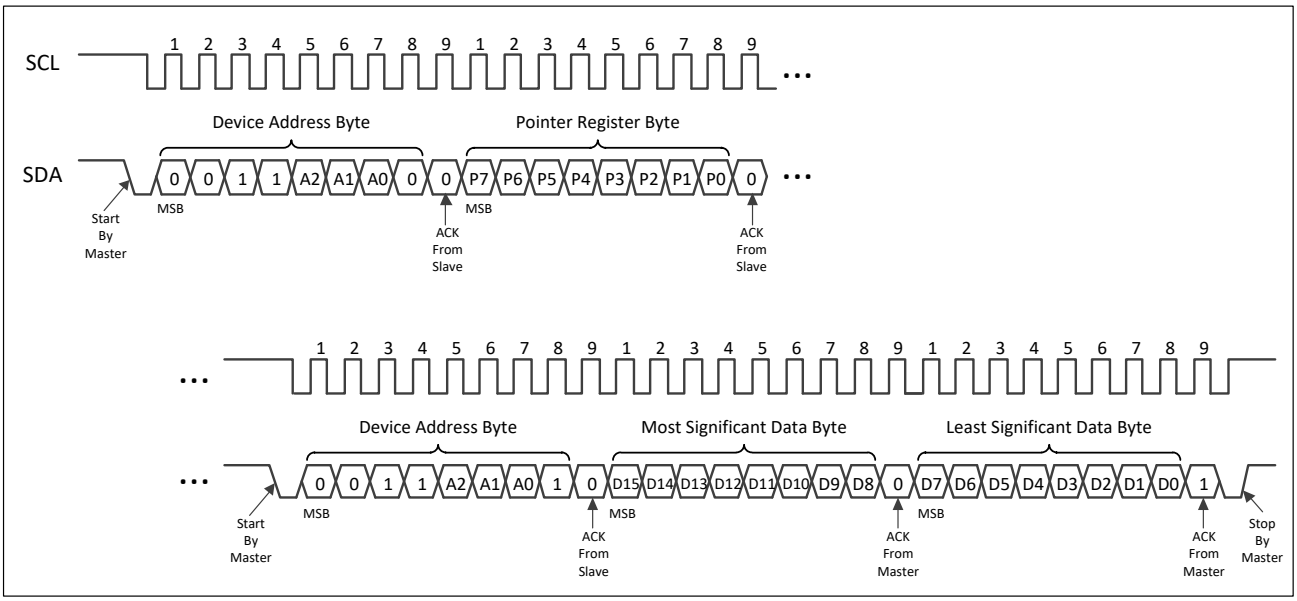


Figure 6–3 I²C Bus Pointer Write Register Word Read



6.3 Temperature Sensor Register Overview

The WB34TS04 contains several registers that are user accessible and/or programmable and utilized for latching the temperature readings, storing high, low and critical temperature limits, configuring the temperature sensor performance, and reporting temperature sensor status.

These registers include a Capability Register, Configuration Register, High Limit Register, Low Limit Register, TCRIT Limit Register, Temperature Data Register, Manufacturer ID Register, Device ID/Revision Register, Temperature Resolution Register and SMBus Timeout Register, as shown in **Table 6–1**.

The WB34TS04 utilizes an Address Pointer Register to access the 16-bit registers. This Pointer Register is an 8-bit Write-only register (see **Table 6–2**). Bit 7 through bit 4 must always be written to '0'. The power-on default value is 00h which is the address location for the Capability Register.

Table 6–1 Temperature Sensor Registers Summary

Address	Read/Write	Register Name	Function	Power-on Default
N/A	$\overline{W}$	Address Pointer	Address storage for subsequent operations	Undefined
00h	R	Capability	Functions and Capability of the temperature sensor	00EFh
01h	R/$\overline{W}$	Configuration	Operation control of the temperature monitor	0000h
02h	R/$\overline{W}$	High Limit	Temperature High Limit	0000h
03h	R/$\overline{W}$	Low Limit	Temperature Low Limit	0000h
04h	R/$\overline{W}$	TCRIT Limit	Critical temperature	0000h
05h	R	Temperature	Current Ambient temperature	N/A
06h	R	Manufacturer ID	PCI-SIG manufacturer ID	104Ah
07h	R	Device ID / Revision	Device ID and Revision number	2201h
08h	R/$\overline{W}$	Temperature Resolution	Selected Temperature Resolution	0001h
09h	R/$\overline{W}$	SMBus Timeout	SMBus Timeout status	0001h
0A-0Fh	R/$\overline{W}$	Vendor-defined	Vendor specific information	N/A

Note: Registers beyond the specified (00-09h) are reserved and must not be accessed by the user in system application, or it may cause undesirable results.

Table 6–2 Address Pointer Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	P4	P3	P2	P1

6.4 Capability Register

The Temperature Sensor Capability Register indicates the supported features of the temperature sensor portion of the WB34TS04. This register is read-only and writing to it will have no effect. **Table 6–3** and **Table 6–4** shows the Capability Register format and bit definition.

Table 6–3 Capability Register Format

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00h	R	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		EVSD	TMOUT	VHV	TRES1	TRES0	RANGE	ACC	EVENT

Table 6–4 Capability Register Bit Definition

Bit	Symbol	Definition
15:8	RFU	Reserved for Future Use. These bits will always read ‘0’.
7	EVSD	$\overline{\text{EVENT}}$ Output with Shutdown Action: 1 = The $\overline{\text{EVENT}}$ pin output is de-asserted (not driven) when entering Shutdown Mode and will remain de-asserted upon exit from Shutdown Mode until the next temperature measurement sample is taken. In Interrupt Mode, the $\overline{\text{EVENT}}$ pin maybe asserted when existing Shutdown if a pending Interrupt has not been cleared.
6	TMOUT	Bus Timeout Period during Normal Operation: 1 = Bus Timeout supported within the range 25ms to 35ms 0 = Bus Timeout is disabled
5	VHV	SA0 Pin High Voltage: 1 = The SA0 pin supports a maximum voltage up to 10V
4:3	TRES[1:0]	Temperature Resolution: 00 = 9-bit, 0.5 °C/LSB 01 = 10-bit, 0.25 °C/LSB (default resolution) 10 = 11-bit, 0.125 °C/LSB 11 = 12-bit, 0.0625 °C/LSB
2	RANGE	Supported Temperature Range: 1 = Temperatures below 0 °C can be read and the Sign bit will be set accordingly
1	ACC	Supported Temperature Accuracy: 1 = Supports a B-grade accuracy of ± 1°C over the active range (75°C to 95°C) and ± 2°C over the monitor range (40°C to 125°C).
0	EVENT	Interrupt Capability: 1 = The device supports Interrupt Capability

6.5 Configuration Register

The Temperature Sensor Configuration Register holds the control and status bits of the $\overline{\text{EVENT}}$ output pin as well as general hysteresis on all limits. To avoid glitches on the $\overline{\text{EVENT}}$ output pin, users should disable EVENT or TCRIT functions prior to programming or changing other device configuration settings. **Table 6–5** and **Table 6–6** shows the Capability Register format and bit definition.

Table 6–5 Configuration Register Formt

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01h	$\overline{\text{R/W}}$	RFU	RFU	RFU	RFU	RFU	HYST1	HYST0	SHDN
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		TCRIT _LOCK	EVENT _LOCK	CLEAR	EVENT _STS	EVENT _CTRL	TCRIT _ONLY	EVENT _POL	EVENT _MODE

Table 6–6 Configuration Register Bit Definition

Bit	Symbol	Definition
15:11	RFU	Reserved for Future Use and must be Logic 0. These bits will always read ‘0’ and writing to them will have no effect. For future compatibility, all RFU bits must be programmed as ‘0’.
10:9	HYST[1:0]	Applied Hysteresis (see **Table 6–7** and **Figure 6–4**) : 00 = Hysteresis is disabled (default) 01 = Hysteresis is enabled at 1.5 °C 10 = Hysteresis is enabled at 3 °C 11 = Hysteresis is enabled at 6 °C This hysteresis applies to all limits when the temperature is dropping below the threshold so that once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. The hysteresis is also applied to $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits is set (bit 7 and bit 6), these bits cannot be altered.
8	SHDN	Shutdown Mode: 0 = The thermal sensor is active and converting (default) 1 = The thermal sensor is disabled and will not generate interrupts or update the temperature data The thermal sensing device and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set (bit 7 and bit 6), this bit cannot be set until unlocked. However it can be cleared at any time. When in shutdown mode, the device still responds to commands normally, however bus timeout may or may not be supported in this mode.
7	TCRIT_LOCK	Locks the TCRIT Limit Register: 0 = The TCRIT Limit Register can be updated normally (default) 1 = The thermal sensor is disabled and will not generate interrupts or update the temperature data
6	EVENT_LOCK	Locks the High and Low Limit Registers: 0 = The High and Low Limit Registers can be updated normally (default) 1 = The thermal sensor is disabled and will not generate interrupts or update the temperature data
5	CLEAR	Clears the $\overline{\text{EVENT}}$ pin asserted: 1 = The $\overline{\text{EVENT}}$ pin is released and will not be asserted until a new interrupt condition occurs This bit is ignored if the device is operating in Comparator Mode. This bit is self-clearing and write only and will always read ‘0’.
4	EVENT_STS	$\overline{\text{EVENT}}$ pin asserted status: 0 = The $\overline{\text{EVENT}}$ pin is not being asserted by the device (default) 1 = The $\overline{\text{EVENT}}$ pin is being asserted by the device

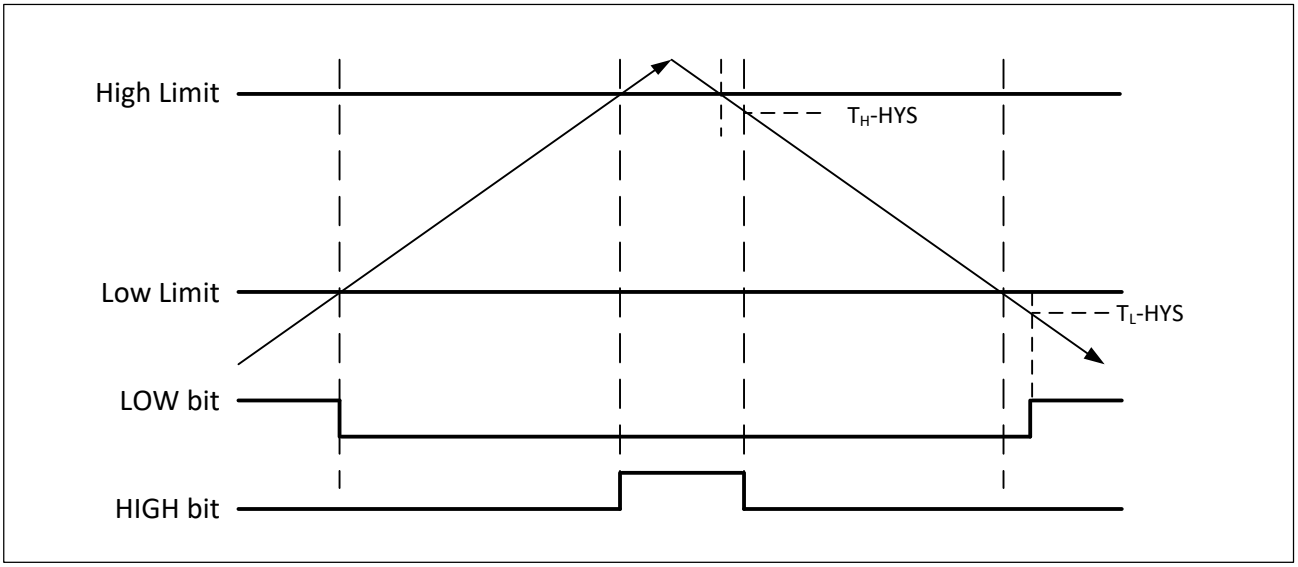
Bit	Symbol	Definition
3	EVENT_CTRL	Masks the $\overline{\text{EVENT}}$ pin from generating an interrupt: 0 = The $\overline{\text{EVENT}}$ pin is disabled and will not generate interrupts (default) 1 = The $\overline{\text{EVENT}}$ pin is enabled If either of the lock bits is set (bit 7 and bit 6), then this bit cannot be altered.
2	TCRIT_ONLY	$\overline{\text{EVENT}}$ pin asserted from a high / low out-of-limit condition: 0 = The $\overline{\text{EVENT}}$ pin will be asserted if the measured temperature is above the High Limit or below the Low Limit in addition to if the temperature is above the TCRIT Limit (default) 1 = The $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature is above the TCRIT Limit When the EVENT_LOCK bit is set, this bit cannot be altered.
1	EVENT_POL	"Active" state of $\overline{\text{EVENT}}$ pin asserted: 0 = The $\overline{\text{EVENT}}$ pin is active low; the "active" state of the pin will be Logic 0 (default) 1 = The $\overline{\text{EVENT}}$ pin is active high; the "active" state of the pin will be Logic 1 If either of the lock bits is set (bit 7 and bit 6), then this bit cannot be altered.
0	EVENT_MODE	$\overline{\text{EVENT}}$ pin function mode: 0 = The $\overline{\text{EVENT}}$ pin will function in comparator mode (default) 1 = The $\overline{\text{EVENT}}$ pin will function in interrupt mode If either of the lock bits is set (bit 7 and bit 6), then this bit cannot be altered.

Table 6–7 Hysteresis as Applied to Temperature Movement

	Below alarm window bit		Above alarm window bit	
	Temperature slope	Temperature threshold	Temperature slope	Temperature threshold
Sets	Falling	T_L[1]-HYS	Rising	T_H[2]
Clears	Rising	T_L	Falling	T_H-HYS[3]

Notes: [1] T_L = Value Stored in the Low Limit Register
[2] T_H = Value Stored in the High Limit Register
[3] HSY = Absolute Value of Selected Hysteresis

Figure 6–4 Hysteresis



6.5.1 Event Output Pin Functionality

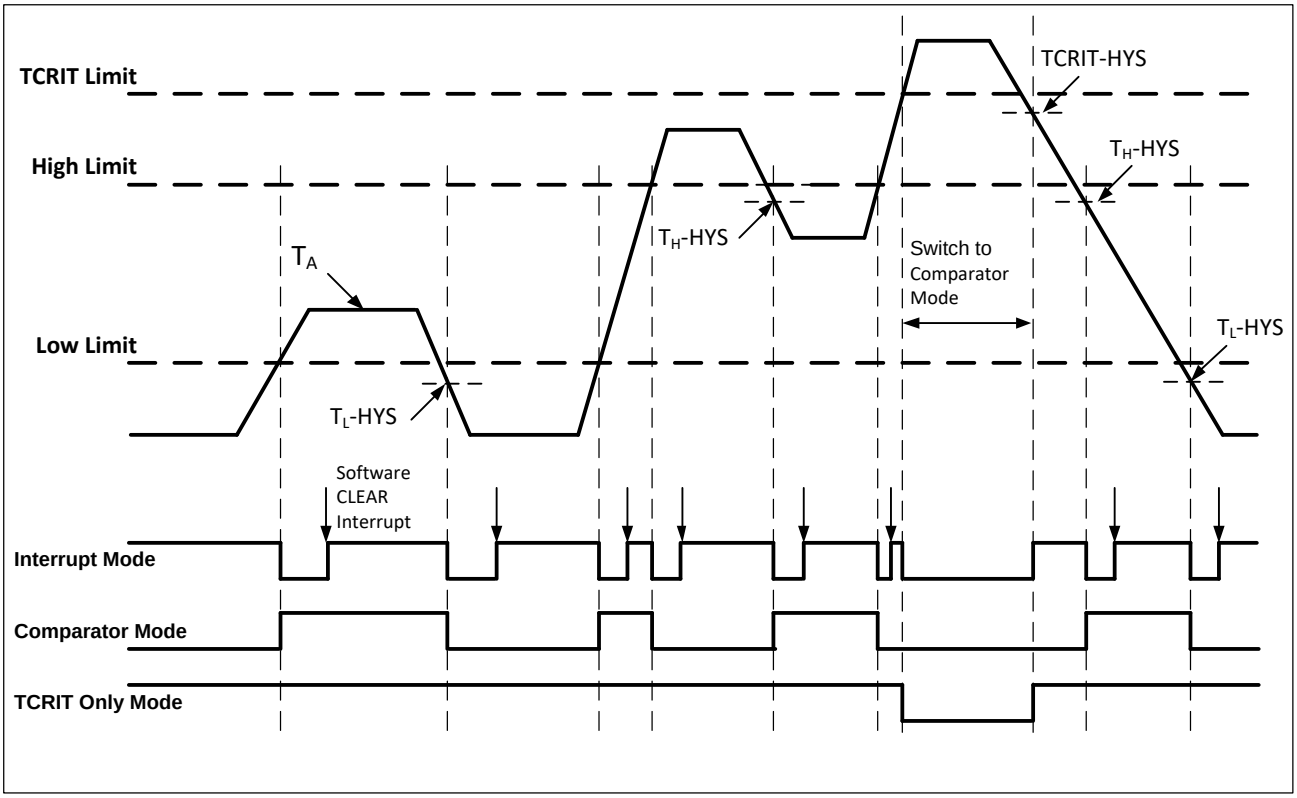
In Interrupt Mode, the $\overline{\text{EVENT}}$ pin will remain asserted until it is released by writing a '1' to the CLEAR bit in the Configuration Register. The value to write is independent of the EVENT_POL bit.

In Comparator Mode, the $\overline{\text{EVENT}}$ pin will clear itself when the error condition that caused the pin to be asserted is removed.

In TCRIT Only Mode, the $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature rises above or equal to the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus TCRIT hysteresis. **Figure 6–5** illustrates the operation of the different modes over time and temperature. Hysteresis will be used to sense temperature movement around trigger points when the HYST1 and HYST0 bits are enabled.

If the device enters the Shutdown Mode with the $\overline{\text{EVENT}}$ pin asserted, the output will be de-asserted. Once the SHDN bit is cleared, the $\overline{\text{EVENT}}$ pin will remain de-asserted until the first temperature conversion (t_{CONV}) is completed. Then, if in Comparator Mode and T_A satisfies the High or Low Limit conditions, the $\overline{\text{EVENT}}$ pin will be asserted; If in Interrupt Mode and the CLEAR bit is never set, the $\overline{\text{EVENT}}$ pin will be re-asserted.

Figure 6–5 $\overline{\text{EVENT}}$ Output Pin Mode Functionality (EVENT_POL = 0, Active Low)



Systems that use the active high mode for $\overline{\text{EVENT}}$ pin must be wired point-to-point between the WB34TS04 and the sensing controller. Wire-OR configuration should not be used with active high $\overline{\text{EVENT}}$ pin since any device pulling the $\overline{\text{EVENT}}$ signal low will mask the other devices on the bus. Also note that the normal state of $\overline{\text{EVENT}}$ in active high mode is a '0', which will constantly draw power through the pull-up resistor.

6.6 Temperature Register Value Definition

Temperatures in the High Limit Register, Low Limit Register, TCRIT Register, and Temperature Data Register are expressed in two's complement format. Bit 12 through bit 2 for each of these registers are defined for all device resolutions as defined in the TRES field of the Capability Register; hence, a 0.25 °C minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits are shown in **Table 6–8**.

Table 6–8 Temperature Register Coding Examples

Bit 15 ~ Bit 0	Value	Unit
xxx0 0000 0010 11xx	+2.75	°C
xxx0 0000 001 00xx	+1.00	°C
xxx0 0000 0000 01xx	+0.25	°C
xxx0 0000 0000 00xx	0	°C
xxx1 1111 1111 11xx	-0.25	°C
xxx1 1111 1111 00xx	-1.00	°C
xxx1 1111 1101 01xx	-2.75	°C

The TRES field of the Capability Register optionally defines higher resolution devices. For compatibility and simplicity, this additional resolution affects both the Temperature Data Register and temperature limit registers. When higher resolution devices generate status or $\overline{\text{EVENT}}$ changes, only bit 12 through bit 2 are used in the comparison; however, all 11 bits (TRES[1:0] = 10) or all 12 bits (TRES[1:0] = 11) are visible in reads from the Temperature Data Register.

When a lower resolution device is indicated in the Capability Register (TRES[1:0] = 00), the finest resolution supported is 0.5 °C. When this is detected, bit 2 of all Limit Registers should be programmed to 0 to assure correct operation of the temperature comparators.

6.7 High Limit Register

The temperature limit registers (High, Low, and TCRIT) define the temperatures to be used by various on-chip comparators to determine device temperature status and thermal EVENTs. For future compatibility, unused bits must be programmed as '0'.

The High Limit Register holds the High Limit for the nominal operating window. When the temperature rises above the High Limit or drops below or equal to the High Limit, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register, then this register becomes Read-only. **Table 6–9** shows the High Limit Register format.

Table 6–9 High Limit Register Format

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
02h	R/$\overline{\text{W}}$	-	-	-	Sign	128	64	32	16
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		8	4	2	1	0.5	0.25	-	-

6.8 Low Limit Register

The Low Limit Register holds the lower limit for the nominal operating window. When the temperature drops below the Low Limit or rises up to meet or exceed the Low Limit, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register, then this register becomes Read-only. **Table 6–10** shows the Low Limit Register format.

Table 6–10 Low Limit Register Formt

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
03h	R/$\overline{\text{W}}$	-	-	-	Sign	128	64	32	16
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		8	4	2	1	0.5	0.25	-	-

6.9 TCRIT Limit Register

The TCRIT Limit Register holds the TCRIT Limit. If the temperature rises above or equal to the limit, the $\overline{\text{EVENT}}$ pin will be asserted. It will remain asserted until the temperature drops below the limit minus a hysteresis. If the TCRIT_LOCK bit is set in the Configuration Register, then this register becomes Read-only. **Table 6–11** shows the TCRIT Limit Register format.

Table 6–11 TCRIT Limit Register Formt

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
04h	R/$\overline{\text{W}}$	-	-	-	Sign	128	64	32	16
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		8	4	2	1	0.5	0.25	-	-

6.10 Temperature Data Register

The 16-bit Read-only Temperature Data Register stores the temperature measured by the internal band gap type temperature sensor, as shown in **Table 6–12**. When reading this register, the MSBs (bit 15 to bit 8) are read first, and then the LSBs (bit 7 to bit 0) are read. The result is the current-sensed temperature. The data format is twos complement with one LSB = 0.25°C for the default resolution.

The upper three bits (bit 15, bit 14, and bit 13) of the Temperature Data Register indicates the trip status of the current temperature, as shown in **Table 6–13**, and are not affected by the status of the event or configuration bits. If neither of the above or below values is set, then the temperature is exactly within the user-defined alarm window boundaries.

Table 6–12 Temperature Data Register Format

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
05h	R	TCRIT	HIGH	LOW	Sign	128	64	32	16
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		8	4	2	1	0.5	0.25[1]	0.125[1]	0.0625[1]

Note: [1] Resolution defined based on the value of TRES[1:0] in the Capability Register. Unused/unsupported bits will read as ‘0’.

Table 6–13 Temperature Data Register Bit Definition

Bit	Symbol	Definition
15	TCRIT	0 = The temperature is below the TCRIT Limit Register setting. 1 = The temperature is above or equal to the TCRIT Limit Register setting. This bit will remain set so long as the temperature is above or equal to the TCRIT Limit and will automatically clear once the temperature has dropped below the limit minus the hysteresis.
14	HIGH	0 = The temperature is below or equal to the High Limit Register setting. 1 = The temperature is above the High Limit Register setting This bit will remain set so long as the temperature is above the HIGH Limit. Once set, it will only be cleared when the temperature drops below or equal to the HIGH Limit minus the hysteresis.
13	LOW	0 = The temperature is above or equal to the Low Limit Register setting 1 = The temperature is below the Low Limit Register setting This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis. Once set, it will only be cleared when the temperature meets or exceeds the Low Limit.
12	Sign	Sign bit: 0 = The temperature is greater than or equal to 0°C. 1 = The temperature is less than 0°C.
11:0	TEMP	Temperature bits: The encoding of bit 11 through bit 0 is the same as for the temperature limit registers.

6.11 Manufacturer ID Register

The Manufacturer ID Register holds the PCI-SIG number 104Ah as shown in **Table 6–14**.

Table 6–14 Manufacturer ID Register Format

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
06h	R	0	0	0	1	0	0	0	0
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		0	1	0	0	1	0	1	0

6.12 Device ID / Revision Register

The upper byte of the Device ID / Revision Register is the Device ID and must be 0x22 for the WB34TS04. The lower byte holds the revision value which is 0x01 for the current device. **Table 6–15** shows the Device ID / Revision Register format.

Table 6–15 Device ID / Revision Register Format

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
07h	R	0	0	1	0	0	0	1	0
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		0	0	0	0	0	0	0	1

6.13 Temperature Resolution Register

With the Temperature Resolution Register, a user can program the temperature sensor resolution from 9-12 bits. The power-on default is always 10-bit (0.25 °C/LSB). The selected resolution RES[1:0] is also reflected in bit 4 and bit 3 (TRES[1:0]) of the Capability Register. **Table 6–16** and **Table 6–17** shows the Temperature Resolution Register format and bit definition.

Table 6–16 Temperature Resolution Register Format

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
08h	R/$\overline{W}$	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		RFU	RFU	RFU	RFU	RFU	RFU	RES1	RES0

Table 6–17 Temperature Resolution Register Bit Definition

Bit	Symbol	Definition
15:2	RFU	Reserved for Future Use. These bits will always read as ‘0’.
1:0	RES[1:0]	Temperature Resolution: 00 = 9-bit, 0.5 °C/LSB 01 = 10-bit, 0.25 °C/LSB 10 = 11-bit, 0.125 °C/LSB 11 = 12-bit, 0.0625 °C/LSB

6.14 SMBus Timeout Register

The SMBus Timeout Register allows the user to enable or disable the SMBus timeout feature. Bit7, SMBOUT as shown in **Table 6–18**, configures the SMBus Timeout function. When the SMBOUT is set to ‘1’, the SMBus Timeout function is active. If the SMBOUT is set to ‘0’, the SMBus Timeout is disabled. Other bits of this register are reserved for future use and will always read as ‘0’. The power-on default value of SMBOUT is ‘1’. The SMBOUT is also reflected in bit 6 (TMOUT) of the Capability Register.

Table 6–18 SMBus Timeout Register Format

Address	Read/Write	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
09h	R/$\overline{W}$	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		SMBOUT	RFU	RFU	RFU	RFU	RFU	RFU	RFU

7 SPD EEPROM

7.1 Memory Orgnization

To provide great flexibility and backwards compatibility with the previous generations of SPD devices, the WB34TS04 memory is organized into two independent 2-Kbit memory arrays (Page 0 and Page 1). Each 2-Kbit (256-byte) array is internally organized as two independent blocks of 128 bytes with each block comprised of eight pages of 16 bytes. Including both memory Pages, there are four 128-byte blocks totaling 512 bytes (see **Table 7–1**).

The WB34TS04 utilizes a Set Page Address (SPA) command and Read Page Address (RPA) command to select and verify the desired half of the memory for Write and Read operations. If SPA = 0, the lower 256 bytes (Page 0) of the SPD EEPROM is selected allowing access to Block 0 and Block 1. Alternately, if SPA = 1, the upper 256 bytes (Page 1)of the SPD EEPROM is selected allowing access to Block 2 and Block 3.

Table 7–1 SPA Setting and Memory Organization

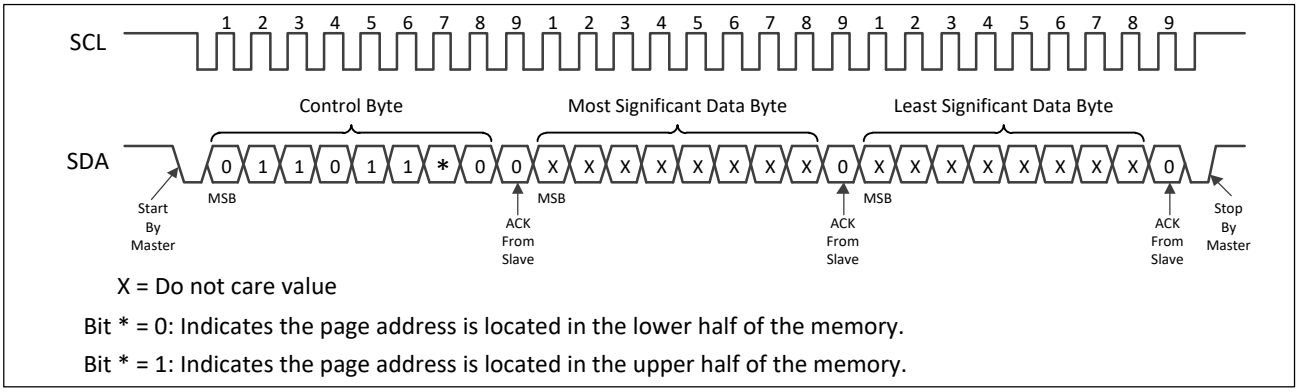
Blocks	Set Page Address (SPA)	Memory Address Locations
Block 0	0	00h to 7Fh (decimal 0 to 127)
Block 1	0	80h to FFh (decimal 128 to 255)
Block 2	1	00h to 7Fh (decimal 0 to 127)
Block 3	1	80h to FFh (decimal 128 to 255)

7.1.1 Set Page Address Command

Setting the SPA value selects the desired half of the SPD EEPROM for Write or Read operation. The SPA command sequence requires the Master to transmit a Start condition followed by sending a control byte of ‘01101100’ or ‘01101110’. ‘0’ in the bit 7 position indicates setting the page address to the lower half of the memory while ‘1’ in this position indicates setting the page address to the upper half of the memory (see **Figure 7–1**). After receiving the control byte, the WB34TS04 should return an ACK and the Master follows by sending two data bytes of Don’t Care values. The WB34TS04 responds with an ACK to each of the two data bytes although the JEDEC TSE2004av specification allows for either an ACK or a NACK response. The protocol is completed by the Master sending a Stop condition.

After power-up, the SPA is set to zero, indicating internal address counter is located in the lower half of the memory. Performing software reset will not change the SPA setting.

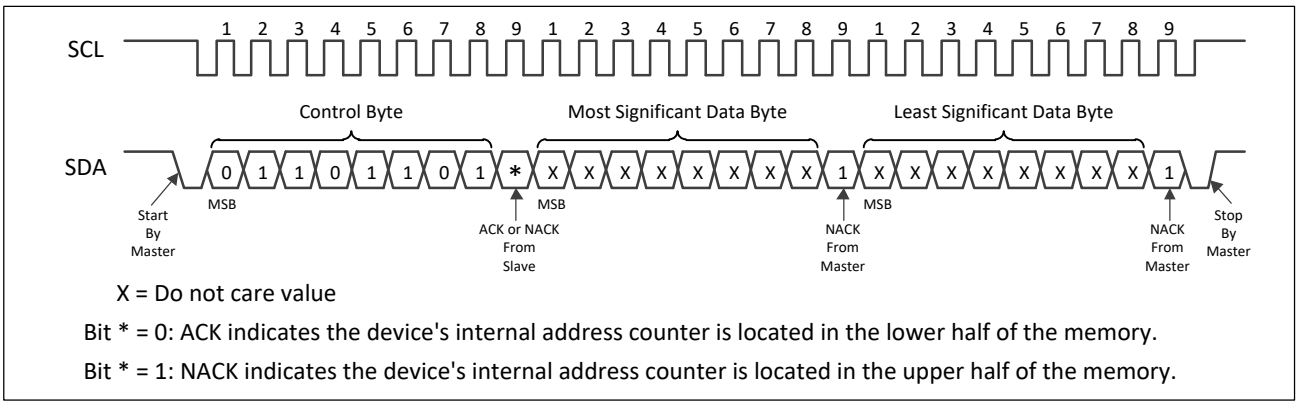
Figure 7–1 Set Page Address (SPA)



7.1.2 Read Page Address Command

Reading the state of the SPA can be accomplished by the RPA command. The RPA command sequence requires the Master to transmit a Start condition followed by a control byte of '01101101'. The Master determines if the internal address counter is located in the lower half or upper half of the memory based on the device's ACK or NACK response. If the device's current address counter is located in the lower half of the memory, the WB34TS04 will respond with an ACK. Alternatively, a NACK response indicates the address counter is located in the upper half of the memory (see **Figure 7–2**). Following the ACK or NACK response, the WB34TS04 transmits two data bytes of Don't Care values. The Master should respond with a NACK on each of the two data bytes followed by sending a Stop condition to end the operation.

Figure 7–2 Read Page Address (RPA)



7.2 Write Operations

The WB34TS04 supports single Byte Write and Page Write up to the maximum page size of 16 bytes in one operation. The only difference between a Byte Write and a Page Write operation is the amount of data bytes sent to the device. Regardless of whether a Byte Write or Page Write operation is performed, the internally self-timed write cycle will take the same amount of time to write the data to the addressed memory location(s).

If a Byte Write or Page Write operation is attempted to a Write Protected or not protected block, the WB34TS04 will respond with ACK or NACK to the write operation according to **Table 7–2**.

Table 7–2 Acknowledge Status When Writing Data or Defining Write Protection

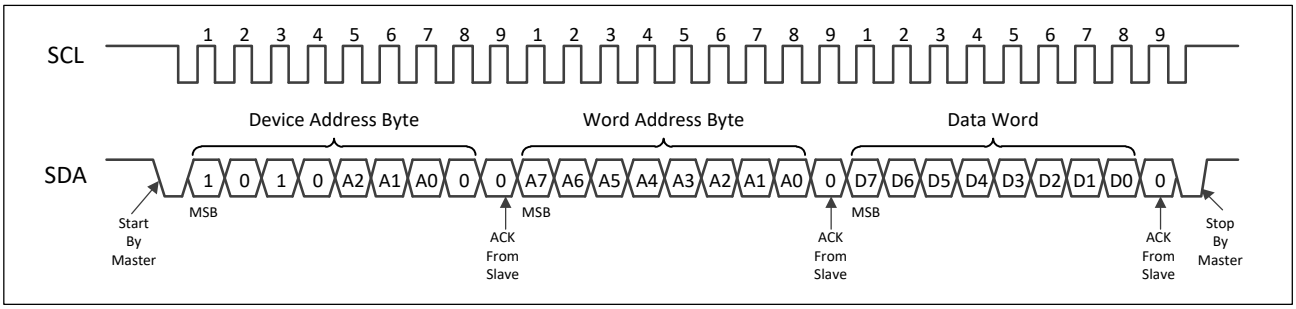
Block Status	Instruction	ACK	Word Address	ACK	Data Word	ACK	Write Cycle
Write Protected	SWPn	NACK	Don't Care	NACK	Don't Care	NACK	No
	CWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write	ACK	Word Address	ACK	Data	NACK	No
Not Protected	SWPn	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	CWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write	ACK	Word Address	ACK	Data	ACK	Yes

7.2.1 Byte Write

For a Byte Write operation, the Master sends a Start condition followed by the device type identifier of '1010', the device address bits and the R/$\overline{W}$ select bit set to Logic 0. The WB34TS04 responds with an ACK during the ninth clock cycle. Then the next byte transmitted by the Master is the 8-bit word address of the byte location to be written into the SPD EEPROM. After receiving an ACK from the WB34TS04, the Master transmits the data word to be programmed followed by an ACK from the WB34TS04. The Master ends the Write sequence with a Stop condition during the 10th clock cycle (see **Figure 7 – 3**) to initiate the internally self-timed write cycle. A Stop condition issued during any other clock cycle during the Write operation will not trigger the internal write cycle.

Once the write cycle begins, the preloaded data word will be programmed in the amount of time not to exceed the t_{WR} specification. During the time, the Master should wait a fixed time by the t_{WR} specification, or for time sensitive applications, an ACK polling routine can be implemented. All inputs are ignored by the device during the write cycle and the device will not respond until the write cycle is complete (see **Figure 7–5**). The SPD EEPROM will increment its internal address counter each time a byte is written.

Figure 7 – 3 Byte Write

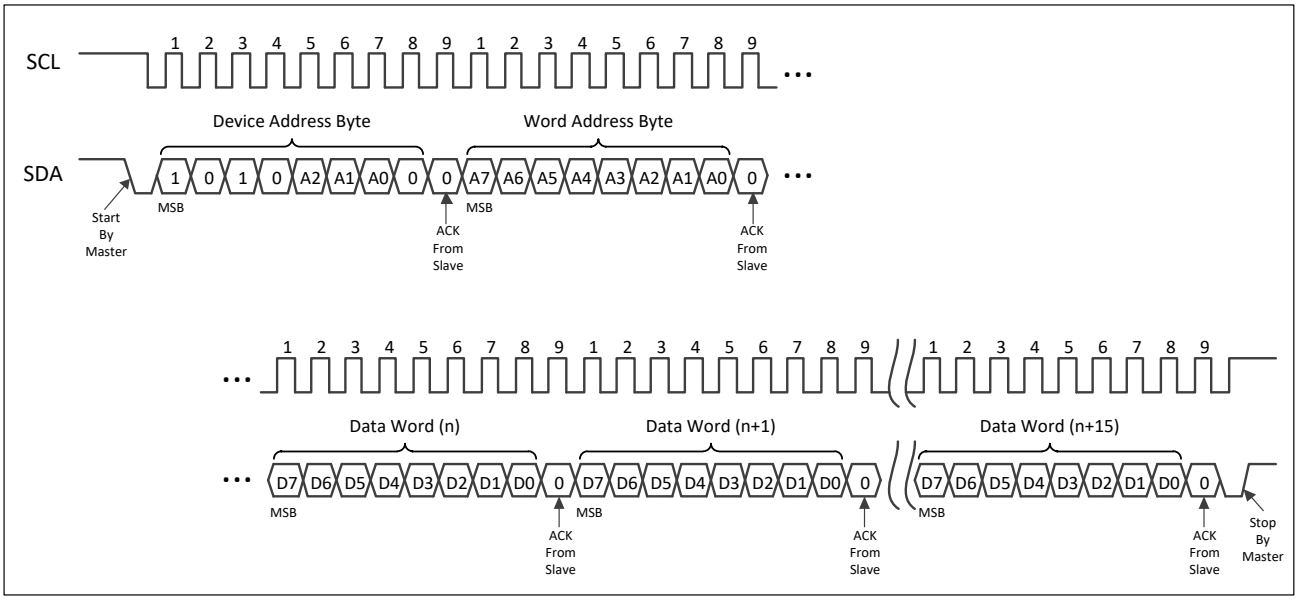


7.2.2 Page Write

The 4-Kbit SPD EEPROM is capable of writing up to 16 data bytes at a time by executing the Page Write protocol sequence. A partial or full Page Write operation is initiated the same as a Byte Write operation except that the Master does not send a Stop condition after the first data word is clocked in. Instead, after the device has acknowledged to the first data word, the Master can transmit up to fifteen more data words. The device will respond with an ACK after each data word is received (see **Figure 7 – 4**). After the device acknowledges to the last data word, the Master should terminate the Page Write sequence with a Stop condition to start the internal write cycle. A Stop condition issued at any other clock cycle will not initiate the internally self-timed write cycle and the Write sequence will have to be repeated again. Once the write cycle begins, the data words should be programmed in the amount of time not exceeding the t_{WR} specification (see **Figure 7–5**). During this time, the Master should wait a fixed time by the specified t_{WR} parameter, or for time sensitive applications, an ACK polling routine can be implemented.

The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, then the following data word is placed at the beginning of the same page. If more than sixteen data words are transmitted to the device, the data word address will roll-over and the previous data will be overwritten. The address roll-over during a Write sequence is from the last byte of the current page to the first byte of the same page.

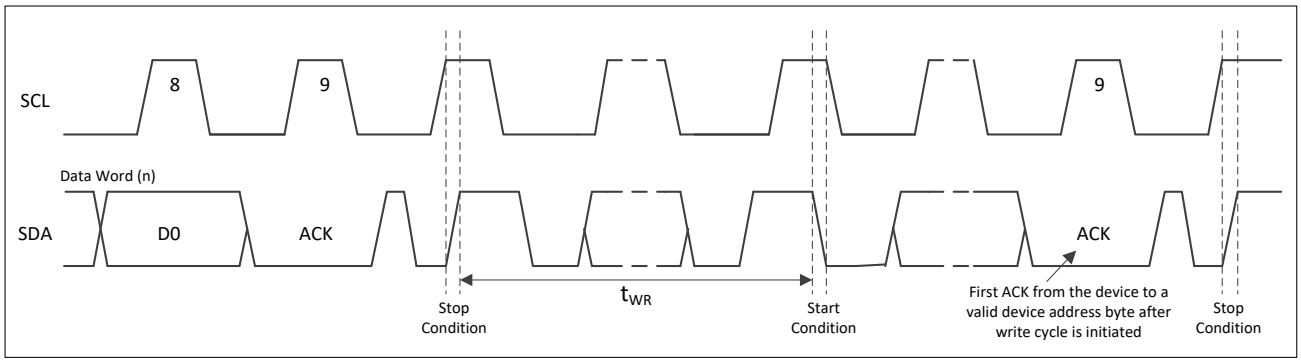
Figure 7－4 Page Write



7.2.3 Write Cycle Timing

The length of the self-timed write cycle, or t_{WR}, is defined as the amount of time from a valid Stop condition that begins the internal write sequence to the Start condition of the first device address byte sent to the WB34TS04 that it subsequently responds with an ACK (see **Figure 7–5**).

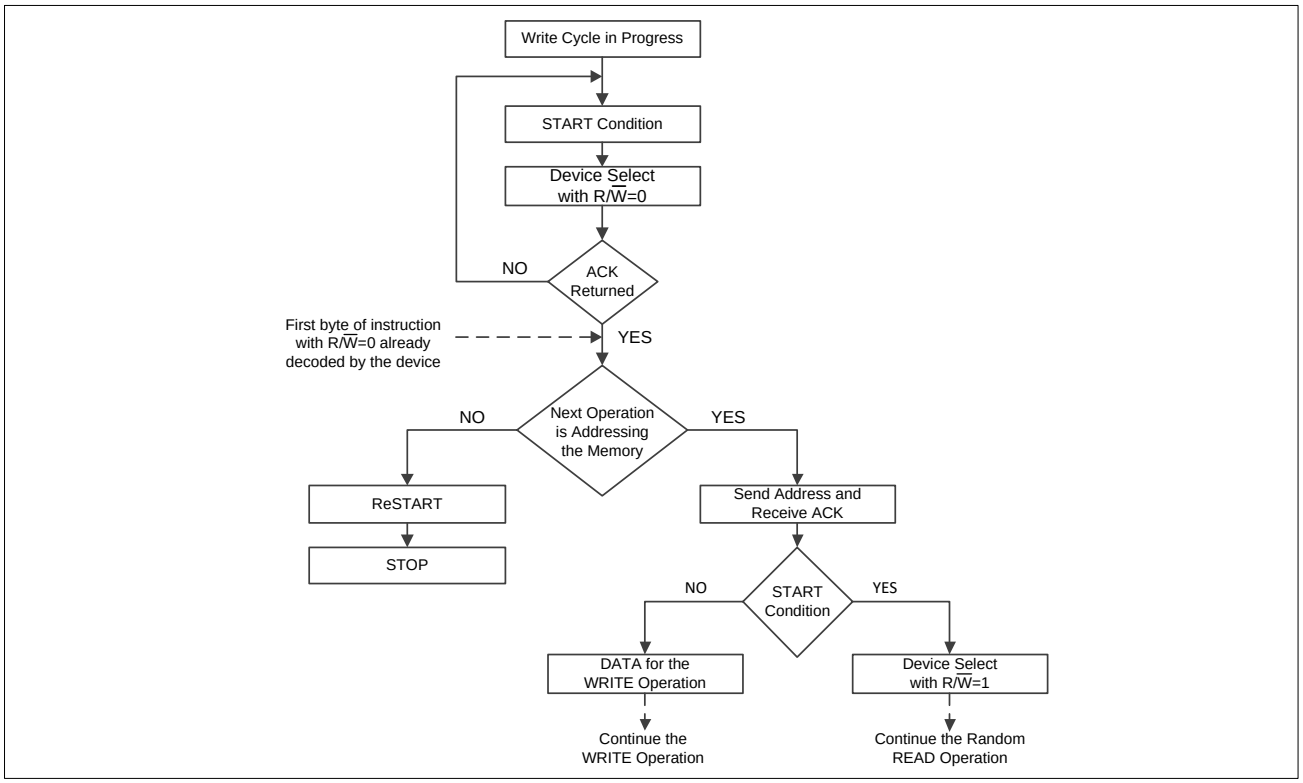
Figure 7–5 Write Cycle Timing



7.2.4 Acknowledge (ACK) Polling

An ACK polling routine can be implemented to optimize time sensitive applications that would not prefer to wait the fixed maximum write cycle time but would prefer to know immediately when the SPD EEPROM write cycle has completed to start a subsequent operation. Once the internally self-timed write cycle has started, the device inputs are disabled and ACK polling can be initiated. An ACK polling routine involves sending a valid Start condition followed by the device address byte. While the write cycle is in progress, the device will not respond with an ACK, indicating the device is busy writing data. Once completed, the device returns an ACK and the next device operation can be started (see **Figure 7–6**).

Figure 7–6 Acknowledge Polling Flow Chart



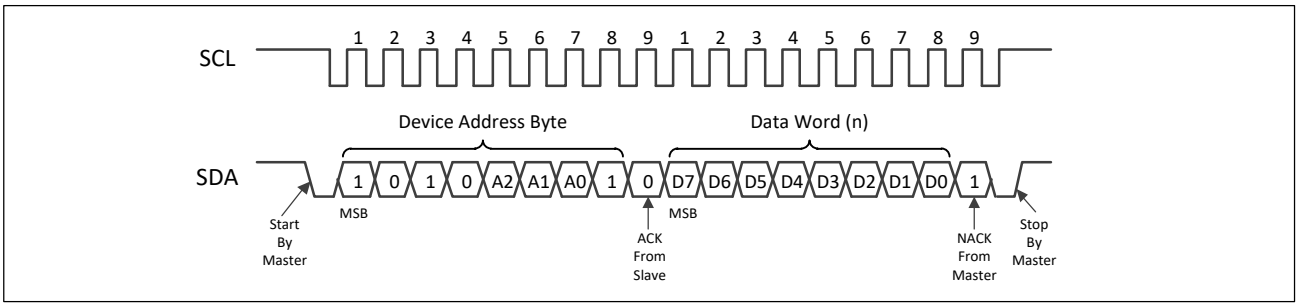
7.3 Read Operations

All Read operations are initiated by the Master transmitting a Start condition, a device type identifier of '1010', three software address bits (A2, A1, A0) corresponding to the hard-wired address pins (SA2, SA1, SA0) and the R/$\overline{W}$ select bit with Logic 1 state. In the following clock cycle, the WB34TS04 should return an ACK. The subsequent sequence depends on the Read operation type. There are three Read operations: Current Address Read, Random Address Read, and Sequential Read.

7.3.1 Current Address Read

For a Current Address Read operation, the Master sends a Start condition followed by transmitting the device address byte with the R/$\overline{W}$ bit set to Logic 1 (see **Figure 7–7**). The WB34TS04 should respond with an ACK and then serially transmits the data word addressed by the internal address counter. This address maintained by the internal address counter is the last address accessed during the last Read or Write operation. The counter is then incremented by one and the address will stay valid between operations as long as power to the device is supplied. The address roll-over during a Read operation is from the last byte of the last memory page to the first byte of the first page. To end the command, the Master responds with a NACK and a Stop condition.

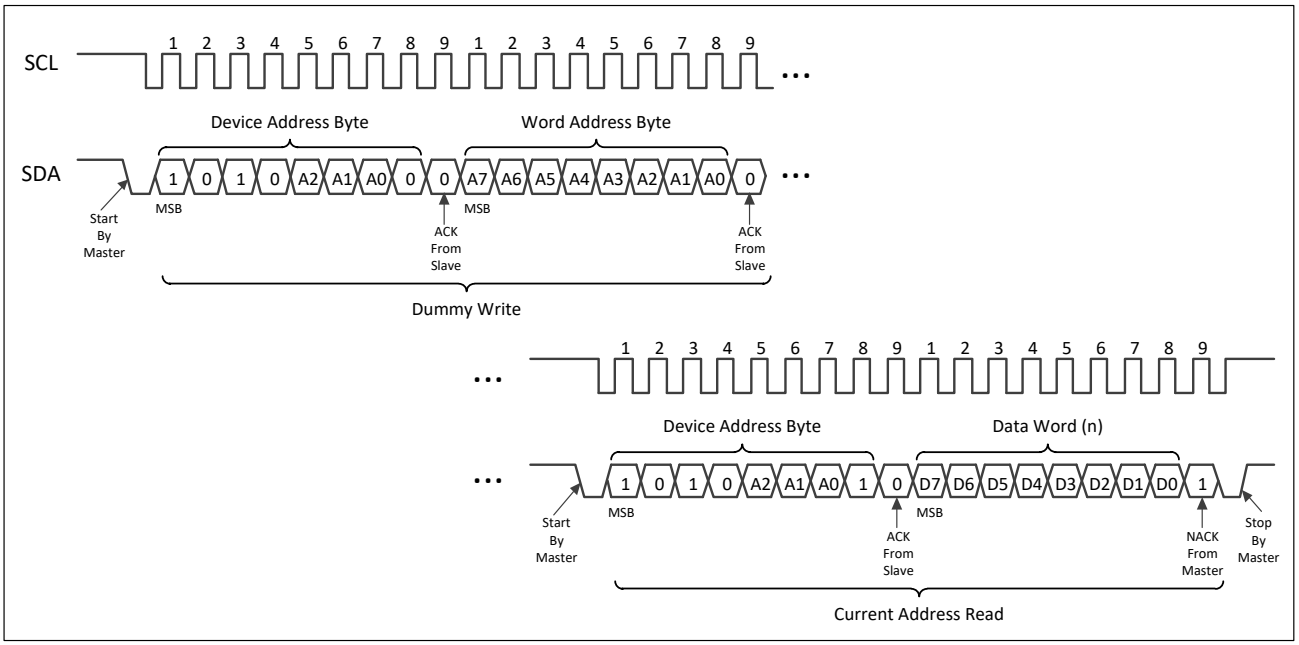
Figure 7–7 Current Address Read



7.3.2 Random Read

A Random Read operation allows the Master to access any memory location in a random manner and requires a dummy write sequence to preload the starting data word address. To perform a Random Read, the device address byte and the word address byte are transmitted to the WB34TS04 as part of the dummy write sequence (see **Figure 7–8**). Once the device address byte and data word address are clocked in and acknowledged by the WB34TS04, the Master generates another Start condition and then initiates a Current Address Read by sending another device address byte with the R/$\overline{W}$ bit set to Logic 1. The WB34TS04 responds with an ACK to the device address byte and serially clocks out the first data word and increments its internal address counter by one. The device will continue to transmit sequential data words as long as the Master continues to ACK each data word. To end the sequence, the Master responds with a NACK followed by a Stop condition.

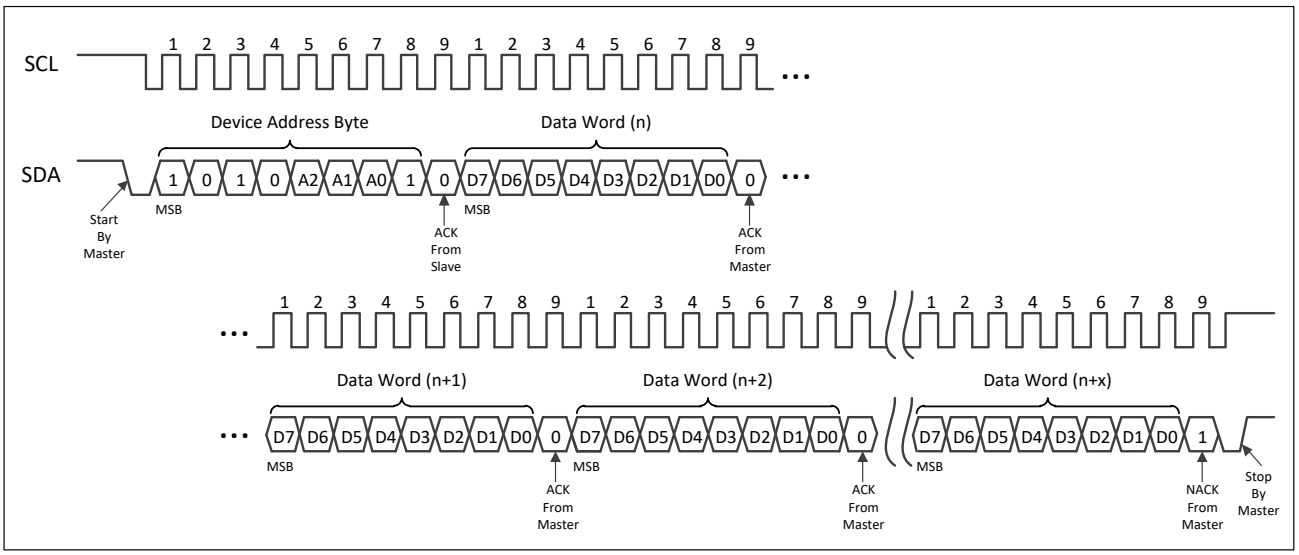
Figure 7–8 Random Read



7.3.3 Sequential Read

A Sequential Read operation is initiated in the same way as either a Current Address Read or a Random Read, except that after transmitted the first data word by the WB34TS04, the Master responds with an ACK instead of a NACK. As long as the WB34TS04 receives an ACK, it will continue to increment the data word address and serially clock out the sequential data words (see **Figure 7–9**). When the internal address counter is at the last byte of the last page, the data word address will roll-over to the first byte of the first page and the Sequential Read operation will continue. The Sequential Read operation is terminated when the Master responds with a NACK followed by a Stop condition.

Figure 7–9 Sequential Read



7.4 Write Protection

The WB34TS04 has three software commands for setting, clearing, or checking the write protection:

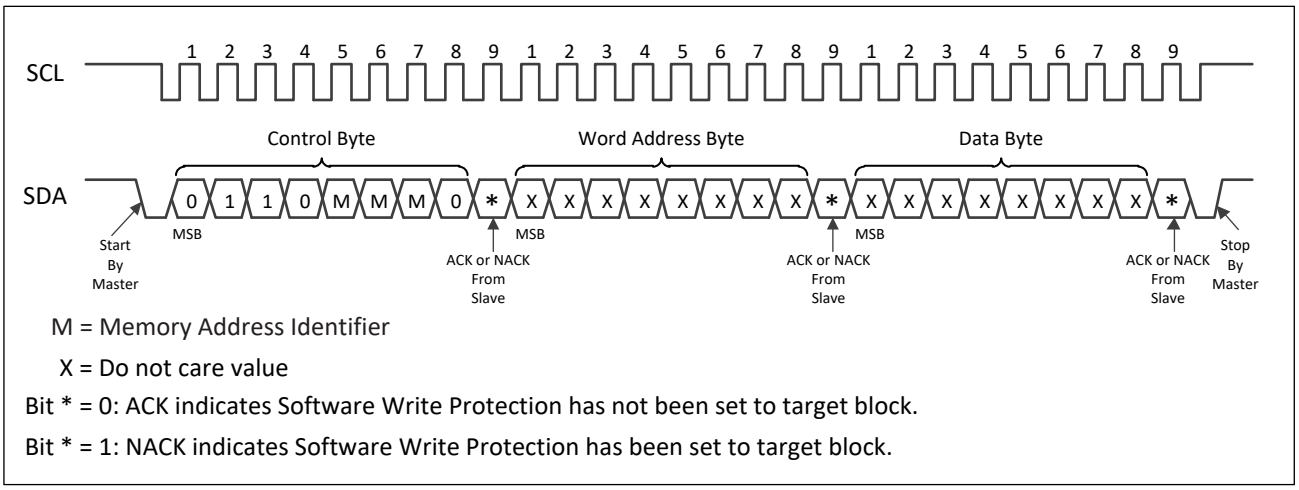
- SWPn: Set Write Protection for Block n
- CWP: Clear Write Protection for all blocks to an unprotected state
- RPSn: Read the Protection Status of Block n

The Software Write Protection feature allows the ability of selective write protection data stored in each of the four independent 128-byte blocks.

7.4.1 Set Write Protection

Setting the Write Protection is enabled by sending the Set Write Protection (SWPn) command to the target Block n. The SWPn sequence requires the Master to send a control byte of '0110MMM0' (where 'M' represents the memory address identifier for the block to be write-protected, see **Table 7–3**) with the R/$\overline{W}$ bit set to Logic 0. If the target block has not been write-protected, the WB34TS04 responds with an ACK to the control byte. If Software Write Protection has been already set to the target block, the WB34TS04 responds with a NACK (see **Table 7–2**). Then the Master transmits a word address byte and a data byte with Don't Care values followed by the WB34TS04 responds to each of the word address byte and the data byte with an ACK or a NACK corresponding to the response on the control byte. To end the SWPn sequence, the Master sends a Stop condition (see **Figure 7–10**). In conjunction with sending the protocol, the SA0 pin must be connected to V_{HV} for the duration of the SWPn sequence. If the SA0 pin is detected not to be connected to V_{HV}, none of the control byte, word address byte and data byte will be acknowledged by the WB34TS04.

Figure 7–10 Set Write Protection



7.4.2 Clear Write Protection

The Write Protection status on all blocks can be reversed by transmitting the Clear Write Protection (CWP) command. The CWP sequence requires the Master to send a Start condition followed by sending a control byte of '01100110' with the R/$\overline{W}$ select bit set to Logic 0. The WB34TS04 should respond with an ACK. Then the Master transmits a word address byte and a data byte with Don't Care values followed by the WB34TS04 responds with an ACK to each of the word address byte and the data byte. To end the CWP sequence, the Master sends a Stop condition (see **Figure 7–11**). In conjunction with sending the protocol, the SA0 pin must be connected to V_{HV} for the duration of CWP command. If the SA0 pin is detected not to be connected to V_{HV}, none of the control byte, word address byte and data byte will be acknowledged by the WB34TS04.

The SWPn acts on a single block only as specified in the SWPn command and can only be reversed by issuing the CWP command and will unprotect all blocks in one operation (see **Table 7–3**). For example, if both Block 0 and Block 3 are needed to be write-protected, two separate SWP0 and SWP3 commands should be required; however, only one CWP command is needed to clear the write protection status of both blocks.

Figure 7–11 Clear Write Protection

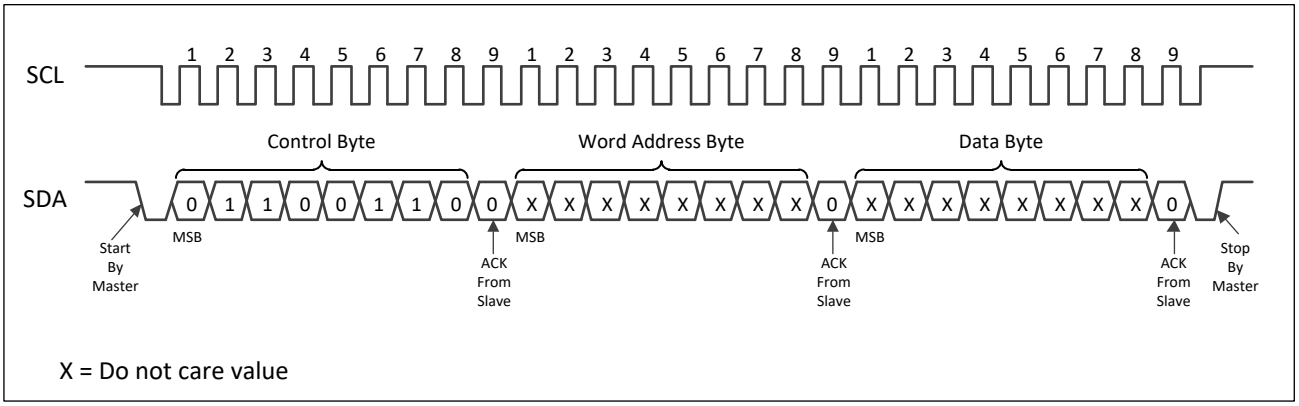


Table 7–3 SWPn, CWP and RPSn

Function	Pin			Control Byte							
				Device Type Identifier				Memory Address Identifier			R/$\overline{W}$
	SA2	SA1	SA0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Set Write Protection, Block 0	X[1]	X	V_{HV}[2]	0	1	1	0	0	0	1	0
Set Write Protection, Block 1	X	X						1	0	0	0
Set Write Protection, Block 2	X	X						1	0	1	0
Set Write Protection, Block 3	X	X						0	0	0	0
Clear All Write Protection	X	X						0	1	1	0
Read Protection Status, Block 0	X	X	0, 1 or V_{HV}	0	1	1	0	0	0	1	1
Read Protection Status, Block 1	X	X						1	0	0	1
Read Protection Status, Block 2	X	X						1	0	1	1
Read Protection Status, Block 3	X	X						0	0	0	1

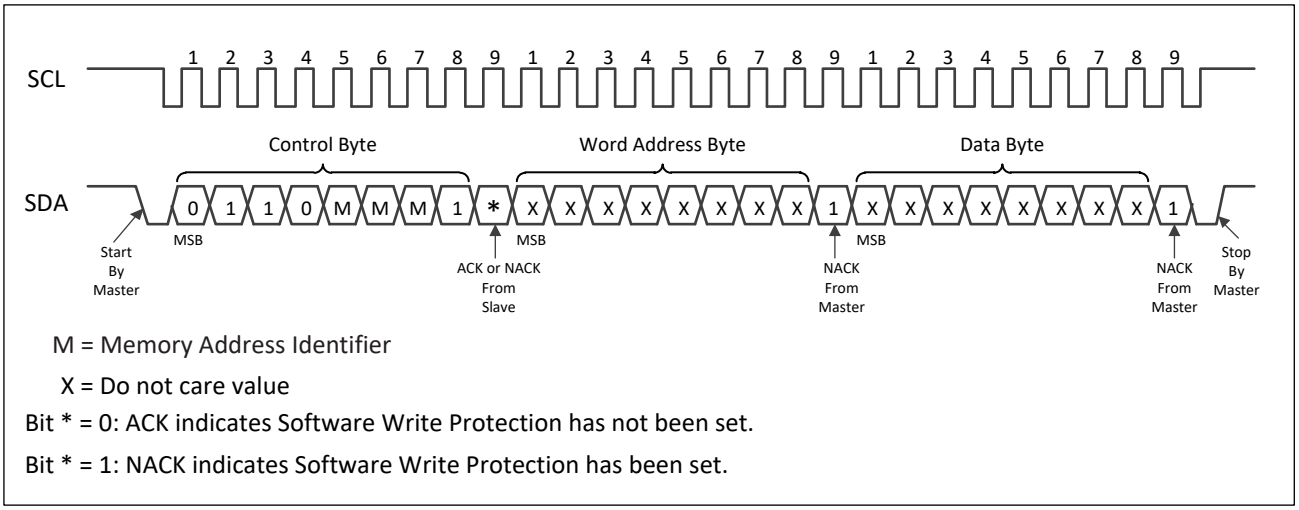
Notes: [1] X = Don't care but recommended to be hard-wired to V_{CC} or GND.

[2] See **Table 8–2** for V_{HV} value.

7.4.3 Read Protection Status

The Read Protection Status (RPSn) command allows the ability to check a block's write protection status. To find out if the Software Write Protection has been set to a specific Block n, the same procedure used to set the block's write protection can be utilized except that the R/$\overline{W}$ select bit is set to Logic 1, and the SA0 pin is not required to be connected to V_{HV}. The RPSn sequence requires the master to send a control byte of '0110MMM1' (where 'M' represents the memory address identifier for the block to be read) with the R/$\overline{W}$ bit set to Logic 1 (see **Table 7–3**). If Software Write Protection has not been set to the target block, the WB34TS04 responds to the control byte with an ACK. Alternately, If Software Write Protection has been set, the WB34TS04 responds with a NACK. In either case, neither the word address byte nor the data byte with Don't Care values will be acknowledged (see **Figure 7–12**). The operation is completed by the Master creating a Stop condition.

Figure 7–12 Read Protection Status



8 Electrical Specifications

8.1 Absolute Maximum Ratings

Table 8–1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient temperature with power applied	-40 to +125	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Supply voltage	-0.5 to +4.3	V
V_{SA0}	Voltage on Pin SA0	-0.5 to +10	V
V_{IN}	Voltage on input Pins	-0.5 to +4.3	V

Note: Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.2 DC Characteristics

Operating range: T_A = -40°C to +125°C, V_{CC} = 1.7V to 3.6V (unless otherwise noted).

Table 8–2 DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{CC}	Supply Voltage		1.7	3.6	V
I_{CC1}	Supply Current, Read Operation	V_{CC}= 3.6V, f_C = 1MHz	-	0.5	mA
I_{CC2}	Supply Current, Write Operation[1]	V_{CC}= 3.6V, f_C = 1MHz	-	1	mA
I_{SB1}	Standby Supply Current	TS Active , EEPROM Standby	-	200	µA
I_{SB2}	Shutdown Supply Current	TS Shutdown , EEPROM standby	-	5	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	-	± 5	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND or V_{CC}, SDA in Hi-Z	-	± 5	µA
V_{IL}	Input Low Voltage (SDA, SCL)		-0.5	0.3*V_{CC}	V
V_{IH}	Input High Voltage (SDA, SCL)		0.7*V_{CC}	V_{CC}+0.5	V
V_{HV}	SA0 Pin High Voltage	V_{HV} – V_{CC} ≥ 4.8V	7	10	V
V_{OL1}	Output Low Voltage[2] Open-drain or Open-collector	V_{CC} > 2V, I_{OL}= 3mA	-	0.4	V
V_{OL2}		V_{CC} ≤ 2V, I_{OL}= 2mA	-	0.2*V_{CC}	V
I_{OL}	Low-Level Output Current[3]	V_{OL} = 0.4V	3.0	20	mA
		V_{OL} = 0.6V	6.0	-	mA
V_{HYST}	Input Hysteresis	V_{CC} < 2V	0.1*V_{CC}	-	V
		V_{CC} ≥ 2V	0.5* V_{CC}		

Notes: [1] This parameter is ensured by design and characterization only.

[2] The same resistor value to drive 3mA at 3.0V V_{CC} provides the same RC time constant when using < 2V V_{CC} with a smaller current draw.

[3] In order to drive full bus load at 400KHz, 6mA I_{OL} is required at 0.6V V_{OL}. Parts not meeting this specification can still function, but not at 400KHz and 400pF.

8.3 AC Characteristics

Measurement conditions: Input rise and fall time ≤ 50ns

Input pulse voltages: $0.2*V_{CC}$ to $0.8*V_{CC}$

Input and output timing reference voltages: $0.3*V_{CC}$ to $0.7*V_{CC}$

Table 8–3 AC Characteristics

Symbol	Parameter	V_{CC}<2.2V		V_{CC}>=2.2V				Unit
		100kHz		400kHz		1000kHz		
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL	10	100	10	400	10	1,000	kHz
t_{HIGH}	Clock Pulse Width High	4,000	-	600	-	260	-	ns
t_{LOW}[1]	Clock Pulse Width Low	4,700	-	1,300	-	500	-	ns
$t_{TIMEOUT}$[2]	Detect Clock Low Timeout	25	35	25	35	25	35	ms
t_R[3]	SDA Rise Time	-	1,000	20	300	-	120	ns
t_F[3]	SDA Fall Time	-	300	20	300	-	120	ns
$t_{SU.DAT}$	Data In Set-up Time	250	-	100	-	50	-	ns
$t_{HD.DI}$	Data In Hold Time	0	-	0	-	0	-	ns
$t_{HD.DAT}$	Data Out Hold Time	200	3,450	200	900	0	350	ns
$t_{SU.STA}$[4]	Start Condition Setup Time	4,700	-	600	-	260	-	ns
$t_{HD.STA}$	Start Condition Hold Time	4,000	-	600	-	260	-	ns
$t_{SU.STO}$	Stop Condition Setup Time	4,000	-	600	-	260	-	ns
t_{BUF}	Time between Stop Condition and next Start Condition	4,700	-	1,300	-	500	-	ns
t_{WR}	Write Cycle Time	-	3	-	3	-	3	ms

Notes: [1] The WB34TS04 shall not initiate clock stretching, which is an optional I^2C Bus feature.

[2] I^2C bus Masters can terminate a transaction in process and reset device communication on the bus by asserting SCL low for $t_{TIMEOUT,MAX}$ or longer. The WB34TS04 detectes this condition must reset their communication and be able to receive a new Start condition no later than $t_{TIMEOUT,MAX}$; the device will not reset if SCL stretching is less than $t_{TIMEOUT,MIN}$.

[3] Guaranteed by design and characterization, not necessarily tested.

[4] For a re-Start condition, or following a write cycle.

Figure 8–1 Bus Timing

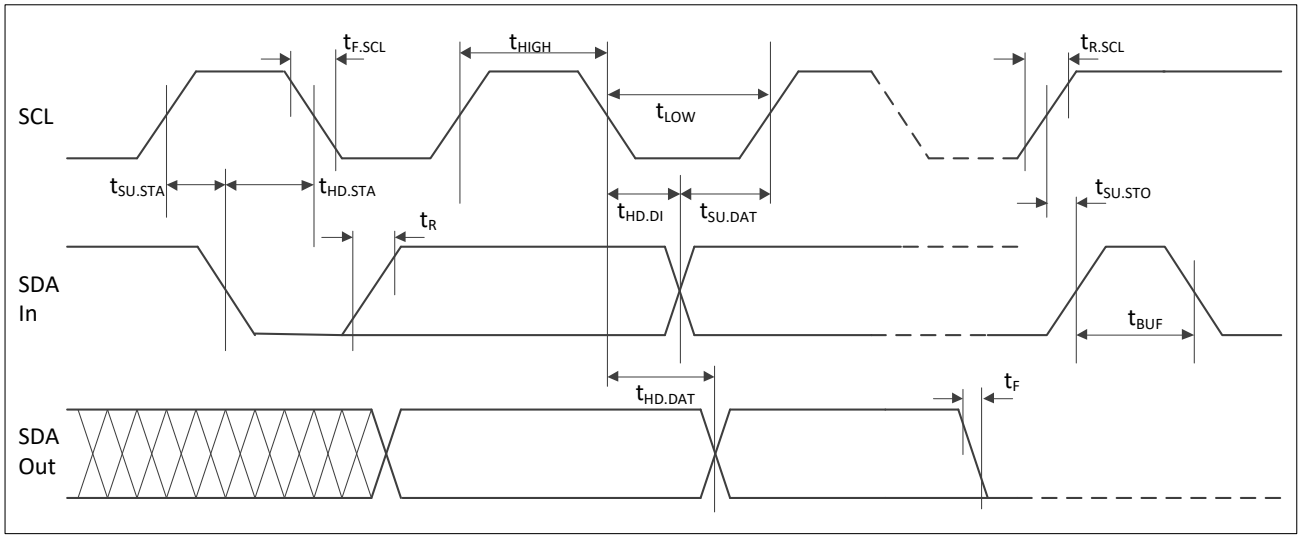
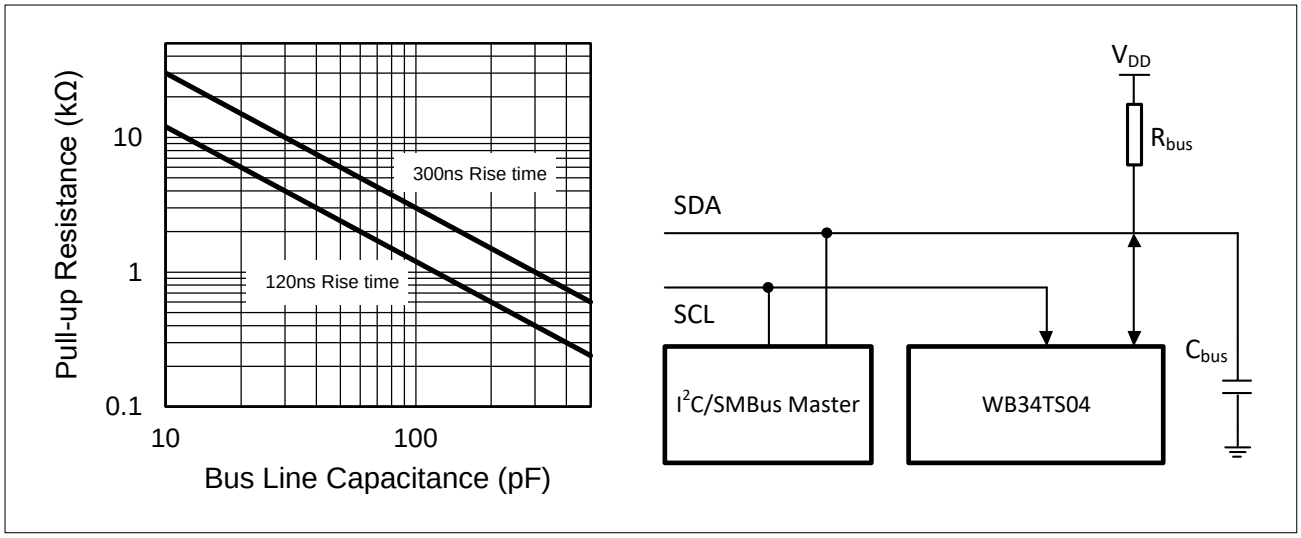


Figure 6–2 Maximum Pull-up Resistance vs. Bus Parasitic Capacitance



8.4 Capacitance

Operating range for pin capacitance: T_A = +25°C, f_C = 400 kHz, V_{CC} = 1.7V to 3.6V.

Table 8–4 Pin Capacitance

Symbol	Parameter[1]	Test Condition	Min	Max	Unit
$C_{I/O}$	Input/output Capacitance (SDA)		-	8	pF
C_{IN}	Input Capacitance (SA0, SA1, SA2, SCL)		-	6	pF
Z_{AIL}	SA0, SA1, SA2 input impedance	V_{IN} < 0.3*V_{CC}	30	-	KΩ
Z_{AIH}	SA0, SA1, SA2 input impedance	V_{IN} > 0.7*V_{CC}	800	-	KΩ
t_{SP}	Pulse width of spikes that must be suppressed by the input filter on SCL and SDA	Single glitch, f_C ≤ 100KHz	-	-	ns
		Single glitch, f_C > 100KHz	0	50	

Note: [1] These parameters are ensured by design and characterization only.

8.5 Temperature to Digital Conversion Performance

Table 8–5 Temperature to Digital Conversion Performance

Symbol	Parameter	Test Condition	Typ[1]	Max	Unit
T_{ACC}	Temperature Sensor Accuracy (B-grade)	+75°C < T_A < +95°C	± 0.5	± 1	°C
		+40°C < T_A < +125°C	± 1	± 2	°C
		-20°C < T_A < +125°C	± 2	± 3	°C
R_{TS}	Temperature Sensor Resolution		0.25	0.0625	°C/LSB
R_{ADC}	ADC Resolution		10	12	bit
t_{CONV}	Conversion Time		70	125	ms

Note: [1] Typical numbers taken at V_{CC} = 3.3V, T_A = 25°C.

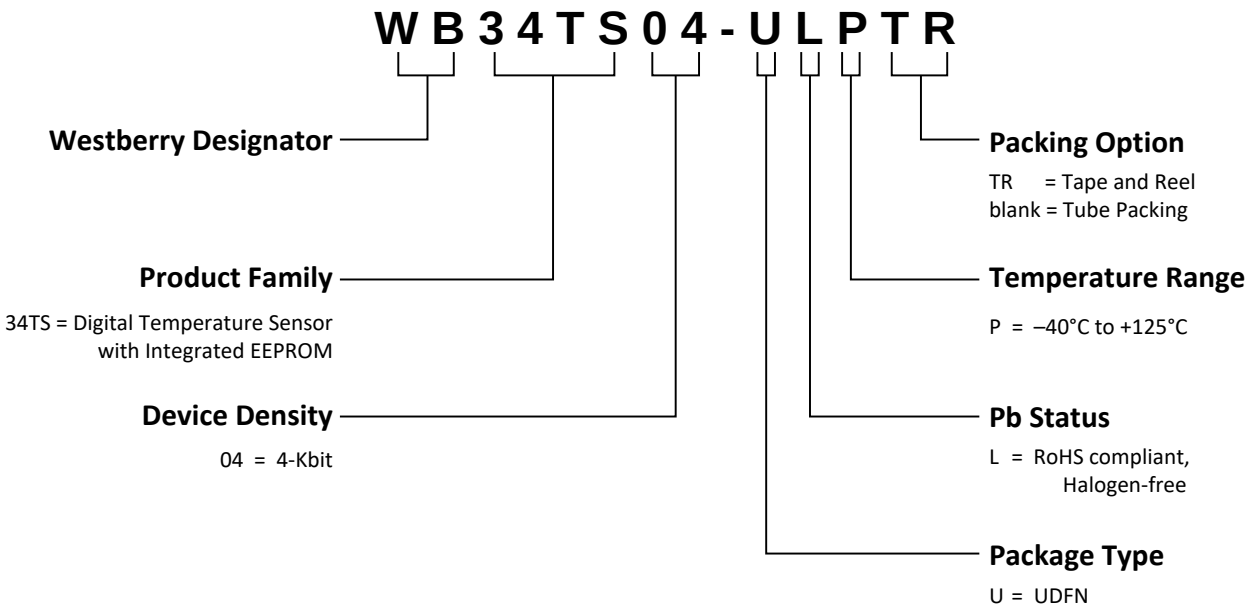
8.6 SPD EEPROM Reliability

Table 8–6 Reliability Performance

Symbol	Parameter	Test Condition	Min	Unit
N_W	Write Cycle Endurance	T_A = +25°C, Page Mode	$2x10^6$	cycle
D_R	Data Retention	T_A = +25°C	200	year

9 Ordering Information

Table 9–1 Ordering information scheme

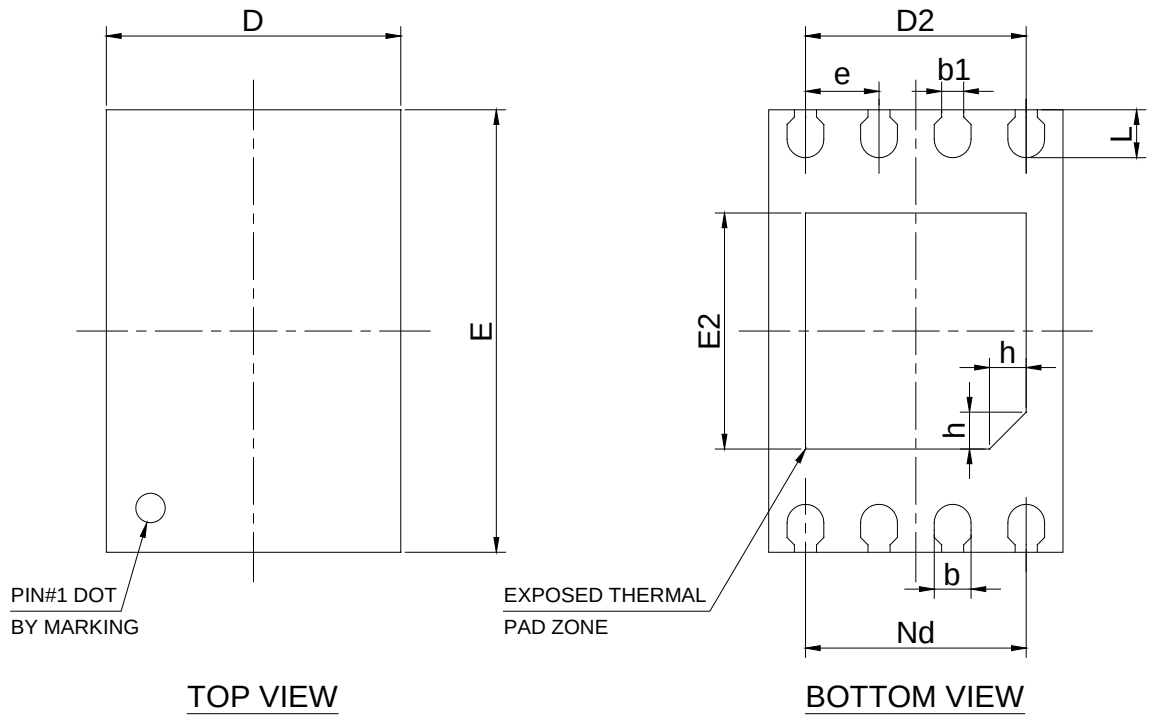


Part Number	Package	Delivery Information	Temperature Range
WB34TS04-ULPTR	2.0 x 3.0mm UDFN	Tape and Reel, 3000 units per Reel	-40°C to +125°C

10 Package Information

10.1 UDFN Package Information

Figure 10–1 8-Lead 2.0 x 3.0mm UDFN Package Outline



SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1	0.16REF		
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.30	0.40	0.50
h	0.20	0.25	0.30

Note:

1. Controlling dimension is mm.
2. Drawing is not to scale.
3. Refer to JEDEC standard MO-229.
4. Default thickness marked by symbol A is 0.55mm (NOM), 0.50mm (NOM) is an alternative if needed.

11 Revision History

Revision	Date	Comments
Rev.1.0	Jan. 2022	Initial version release